DESCRIPTION

The 10155 is a 16-bit ECL Content Addressable Memory (CAM) organized as an array of 8 words by 2 bits. Each cell of the array consists of a D-type latch and an exclusive-OR comparator, along with control logic for reading, writing and masking.

The modes of operation possible with the 10155 are associate, masked associate, read, write, and hybrid. Lines Y_0-Y_7 are used for linear word select in the read/write mode, and are used as outputs for match/mismatch information in the associate mode.

In associate operation, I_0 and I_1contain information to be compared. If the latches at a particular Y location are in a state matching the input data, that Y line goes low.

The Y outputs are open emitters, allowing expansion in multiples of 2 bits by tying additional 10155's to the Y bus lines. To inhibit comparison of a particular bit, the corresponding A_0 or A_1 line is held low.

In the read mode, the state of the selected cells appears on outputs D_0 and D_1. In the write mode, these outputs are transparent, following the state of I_0 and I_1.

In Hybrid mode, one of the I_0 or I_1 data inputs may be associated with the Q_{n0} or Q_{n1} cells respectively. If a match exists, the corresponding Y_n line(s) will go low, and can be used to address the other half of the memory for writing new data. Thus, it is possible to write I_1 in Q_{n1} where I_0 matches Q_{n0} or vice versa.

FEATURES

- **12ns associate time (max.)**
- **Linear address select**
- **Single bit masking**
- **50 Ω output drive**
- **ECL 10K compatible**
- **Open emitter match lines for easy bit expansion**
- **50kΩ input pulldown resistors (except on Y lines)**

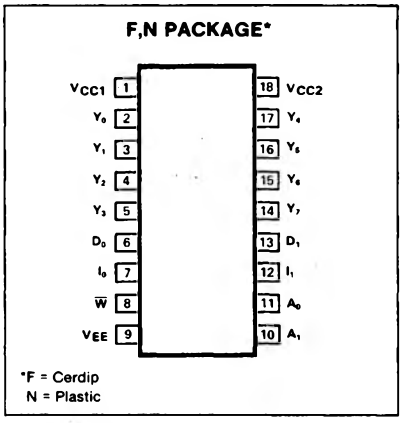
APPLICATION

- **Content addressable memory systems**

RECOMMENDED OPERATING VOLTAGES

- $V_{CC1} = V_{CC2} = 0V$
- $V_{EE} = -5.2V \pm 5\%$

PIN CONFIGURATION



TRUTH TABLE (POSITIVE LOGIC)

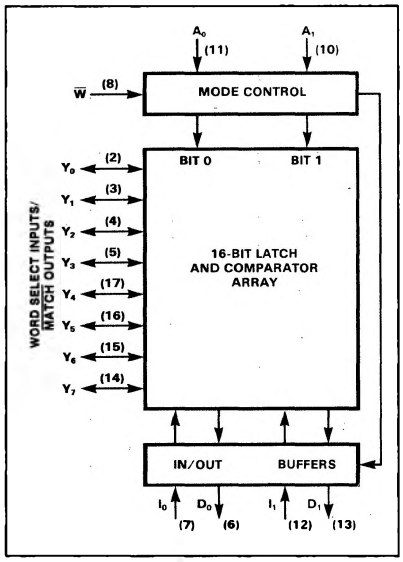
MODE	A_0	A_1	I_0	I_1	$\overline{W}$	D_0	D_1	Q_{n0}	Q_{n1}	Y_n
Associate[1]	1	1	1/0	1/0	X	0	0	Q_{n0}	Q_{n1}	$Q_{n0} \oplus I_0 + Q_{n1} \oplus I_1$
Associate[1,2] (masked)	1	0	1/0	X	1	0	D_1	Q_{n0}	Q_{n1}	$Q_{n0} \oplus I_0$
Associate[1,2] (masked)	0	1	X	1/0	1	D_0	0	Q_{n0}	Q_{n1}	$Q_{n1} \oplus I_1$
Read[3]	0	0	X	X	1	D_0[2]	D_1[2]	Q_{n0}	Q_{n1}	0 (Selected address)
Write[3,4]	0	0	1/0	1/0	0	I_0	I_1	I_0	I_1	0 (Selected address)
Hybrid[5]	1	0	1/0	1/0	0	0	I_1	Q_{n0}	$I_1 \cdot \overline{Y_n}$	$Q_{n0} \oplus I_0$
Hybrid[5]	0	1	1/0	1/0	0	I_1	0	$I_0 \cdot \overline{Y_n}$	Q_{n1}	$Q_{n1} \oplus I_1$

X = Don't care
Q_{n0} = Contents of address n, Bit 0 (n = 0 to 7)
Q_{n1} = Contents of address n, Bit 1

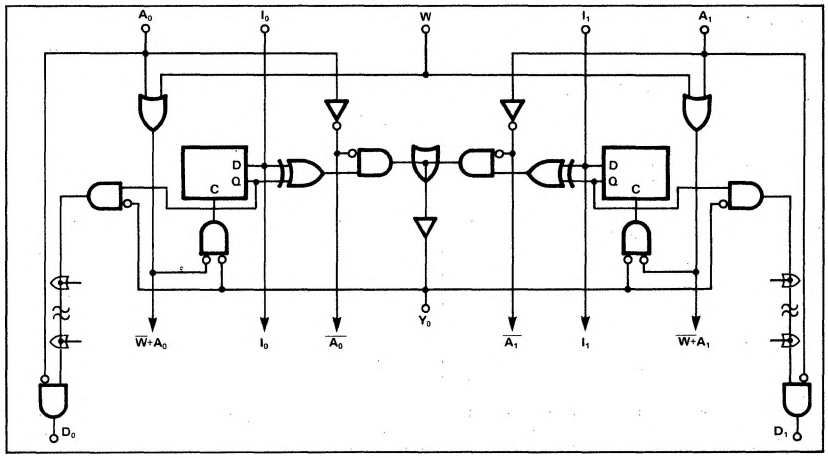
NOTES

1. 1 (high) = Mismatch, 0 (low) = Match
2. Read mode: $D_0 = Q_{00} \cdot \overline{Y_0} + Q_{10} \cdot \overline{Y_1} + \cdots + Q_{70} \cdot \overline{Y_7}$
   $D_1 = Q_{01} \cdot \overline{Y_0} + Q_{11} \cdot \overline{Y_1} \cdots + Q_{71} \cdot \overline{Y_7}$
3. In normal operation a single Y address is selected for read or write
4. Write is transparent
5. Simultaneous Associate and Write at all "Match" addresses.

BLOCK DIAGRAM



LOGIC DIAGRAM (TYPICAL BIT)



ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2} = 0V$

PARAMETER		RATING	UNIT
V_{EE}	Supply voltage	-8	Vdc
V_{IN}	Input voltage	0 to V_{EE}	Vdc
I_O	Output source current	40	mAdc
	Temperature Range		°C
T_A	Operating	-30 to +85	
T_J	Operating junction	125	
T_{STG}	Storage	-55 to +125	

DC ELECTRICAL CHARACTERISTICS[1] $V_{CC1} = V_{CC2} = 0V$, $V_{EE} = -5.2V$, $R_L = 50\Omega$ to $-2V$

PARAMETER		TEST CONDITIONS	-30 °C			+25 °C			+85 °C			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Input voltage											V
V_{IL}	Low		-1.890			-1.850			-1.825			
V_{IH}	High				-0.890			-0.810			-0.700	
V_{ILA}	Low threshold				-1.500			-1.475			-1.440	
V_{IHA}	High threshold		-1.205			-1.105			-1.035			
	Output voltage											V
V_{OL}	Low	V_{IH} = Max, V_{IL} = Min	-1.89		-1.675	-1.65	-1.70	-1.85	-1.825		-1.615	
V_{OH}	High		-1.06		-0.89	-0.96	-0.89	-0.81	-0.89		-0.70	
V_{OLA}	Low threshold				-1.655			-1.63			-1.595	
V_{OHA}	High threshold	V_{IHA} = Min, V_{ILA} = Max	-1.08			-0.98			-0.91			
	Input current											μA
I_{IL}	Low	Y,A,I,W = V_{IL} Min				0.5						
I_{IH}	High	A = V_{IH} Max						220				
		I,W = V_{IH} Max						200				
		Y = V_{IH} Max						50				
I_{EE}	Supply current	V_{IH} Max					115	140				mA

AC ELECTRICAL CHARACTERISTICS[2] $-30°C \le T_A \le +85°C$, $V_{CC1} = V_{CC2} = +2V$, $V_{EE} = -3.2V$, $R_L = 50\Omega$ to ground

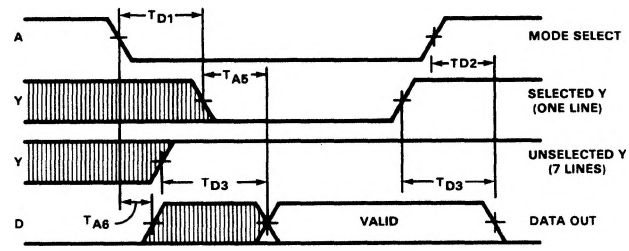
PARAMETER		FROM	TO	TEST CONDITIONS	LIMITS			UNIT
					Min[3]	Typ[4]	Max	
	Associate time							ns
T_{A1}		I±	Y±			8	12	
T_{A2}		A+	Y+			9	12	
	Disable time							ns
T_{D1}		A-	Y-			8	12	
T_{D2}		A+	D-			4	7	
T_{D3}		Y+	D-			9	13	
	Setup and hold time							ns
T_{H1}	Hold time	$\overline{W}$+	A+		1	0		
T_{S2}	Setup time	A-	Y-		15	11		
T_{H2}	Hold time	$\overline{W}$+	Y±		3	1		
T_{S3}	Setup time	Y+	$\overline{W}$-		3	2		
T_{H3}	Hold time	$\overline{W}$+	I±		3	1		
T_{S4}	Setup time	I±	$\overline{W}$+		5	3		
T_W	Write pulse width				10	5		ns
	Access time							ns
T_{A3}	Write	$\overline{W}$-	D±	$T_{S4} \ge T_W$		13	17	
T_{A4}	Write	I+,-	D+,-			9	13	
T_{A5}	Read	Y-	D+			6	10	
T_{A6}	Read	A-	D+			4		

NOTES

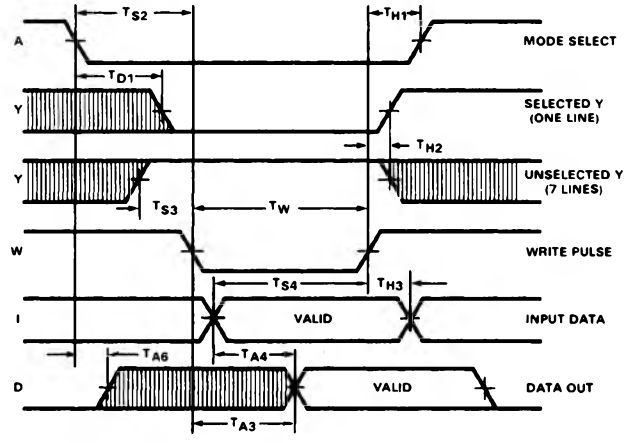
1. Each ECL 10K series device has been designed to meet the dc and ac specifications after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.
2. Refer to dc characteristics.
3. Minimum allowed.
4. All typical values are at $T_A = +25°C$.

VOLTAGE WAVEFORMS

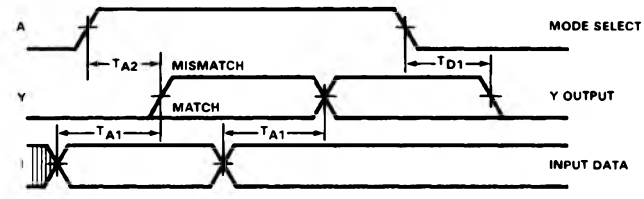
READ CYCLE



WRITE CYCLE



ASSOCIATE CYCLE



MEASUREMENT CIRCUIT