

DESCRIPTION

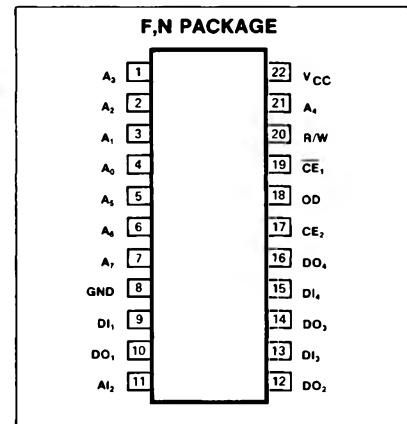
The 2101 series is high performance, low power static read/write RAM's.

The 2101 series is fabricated with n-channel silicon gate technology which allows the design of high performance easy to use MOS circuits and provides a high functional density on a given monolithic chip.

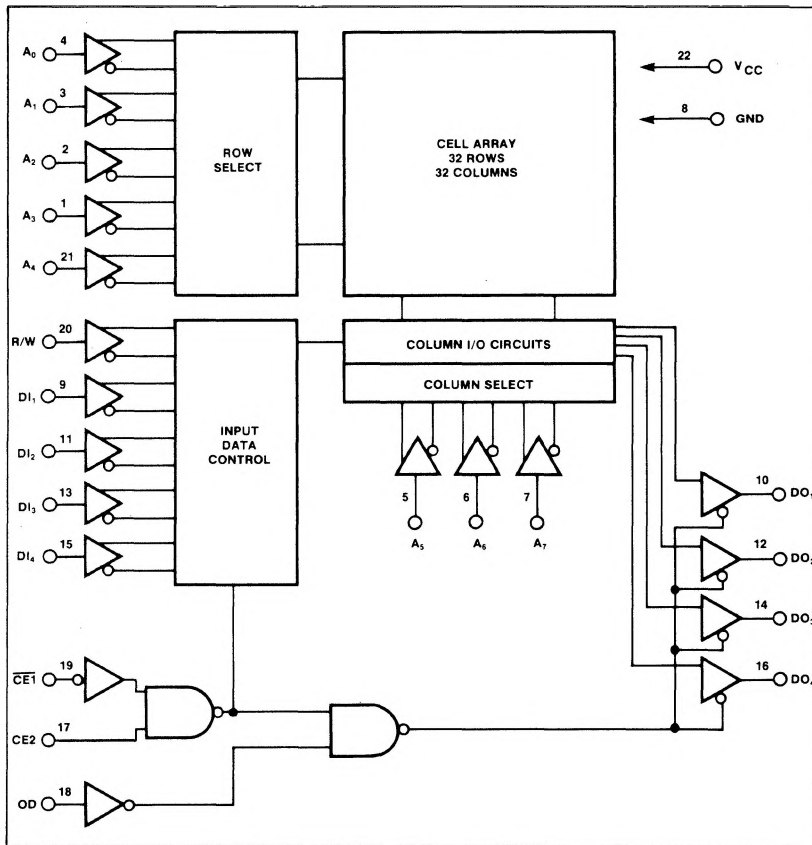
FEATURES

- Fully static
- No refresh operations, sense amps or clocks required
- All inputs and outputs are TTL compatible
- One 5V power supply required

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS¹

PARAMETER	RATING	UNIT
TA Operating under bias	0 to 70	°C
TSTG Storage	-65 to 150	
PD Power dissipation	1	W
Voltage on any pin with respect to ground	-0.5 to 7	V

DC ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$, unless otherwise specified

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ ²	Max	
V_{IL} V_{IH}	Input voltage Low High	-0.5 2.2		0.65 V_{CC}	V
V_{OL} V_{OH}	Output voltage Low High			0.45	V
I_{LI}	Input current	$V_{IN} = 0$ to 5.25V			μA
I_{LOH} I_{LOL}	I/O leakage current ³	$CE_1 = 2.2\text{V}$ $V_{OUT} = 4.0\text{V}$ $V_{OUT} = 0.45\text{V}$			μA
I_{CC1} I_{CC2}	Supply current	$V_{IN} = 5.25\text{V}$, $I_O = 0\text{mA}$ $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$			mA
C_{IN} C_{OUT}	Capacitance ³ Input (All pins) Output	$V_{IN} = 0\text{V}$ $V_{OUT} = 0\text{V}$			pF

AC ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$, Input pulse levels = $+0.65\text{V}$ to 2.2V , Input pulse rise and fall times = 20ns , Timing measurement reference level = 1.5V , Output load = 1 TTL gate and $C_L = 100\text{pF}$, unless otherwise specified.

PARAMETER	TO	FROM	2101			2101-1			2101-2			UNIT	
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{RC}	Output Output High Z state	Chip enable Output disable Data output	READ CYCLE										
t_A			Read cycle	1,000			500			650			ns
t_{CO}			Access time									650	ns
t_{OD}												400	ns
t_{DF}^4												350	ns
t_{OH}	Previous read data valid after change of address		0		200	0		150	0		150	ns	
			40			40			40			ns	
t_{WC}	Write	Chip enable	WRITE CYCLE										
t_{AW}			Write cycle	1,000			500			650			ns
t_{CW}			Write delay	150			100			150			ns
			900			400			550			ns	
t_{DW}	Rise of R/W Change of data in Output	Data in Rise of R/W	Setup and hold time										
t_{DH}			Setup time	700			280			400			ns
t_{DS}			Hold time	100			100			100			
t_{DS}	Setup time		200			150			150				
t_{WP}	Write pulse												
t_{WR}			Write recovery	750			300			400			ns
			50			50			50			ns	

NOTES

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- Typical values are for $T_A = 25^\circ\text{C}$ and typical supply voltage.
- This parameter is periodically sampled and is not 100% tested.
- t_{of} is with respect to the trailing edge of CE_1 , CE_2 or OD , whichever occurs first.
- CD should be tied low for separate I/O operation.

TIMING DIAGRAMS

