

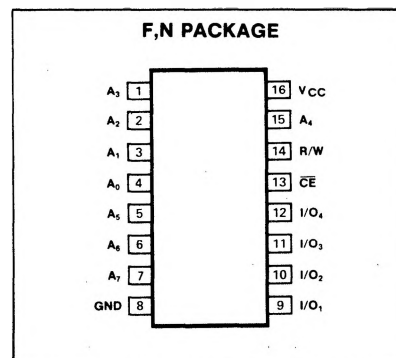
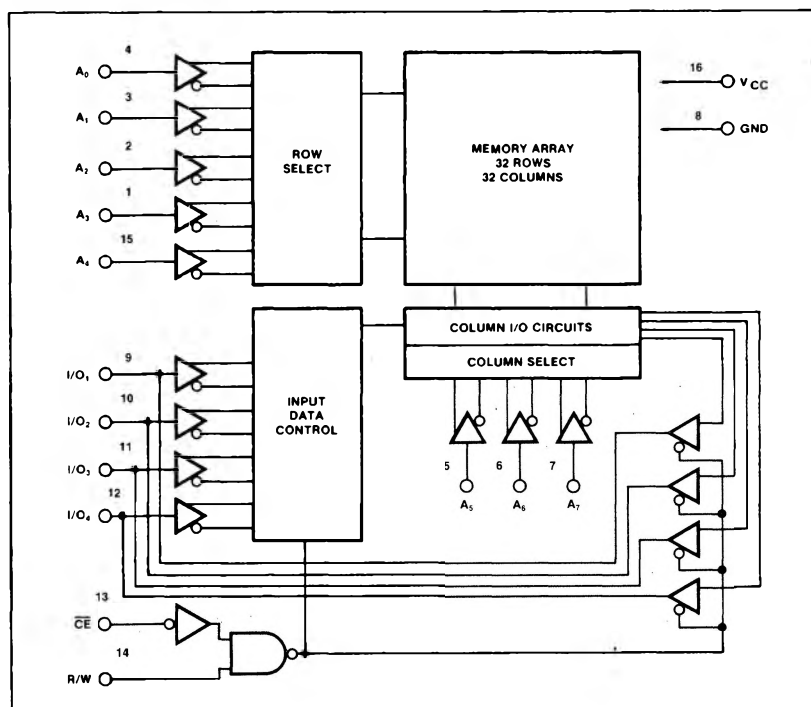
DESCRIPTION

The 2112 series is high performance, low power static read/write RAMs.

The 2112 series is fabricated with n-channel silicon gate technology which allows the design of high performance easy to use MOS circuits and provides a high functional density on a given monolithic chip.

FEATURES

- Fully static
- No refresh operations, sense amps or clocks required
- Directly TTL compatible
- One 5V power supply

PIN CONFIGURATION**BLOCK DIAGRAM****ABSOLUTE MAXIMUM RATINGS¹**

PARAMETER	RATING	UNIT
T_A Temperature range		°C
Operating under bias	0 to 70	
T_{STG} Storage	-65 to 150	
Voltage on any pin with respect to ground	-0.5 to 7	V
P_D Power dissipation	1	W

DC ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ ²	Max	
V_{IL} V_{IH}	Input voltage Low High	-0.5 2.2		0.65 V_{CC}	V
V_{OL} V_{OH}	Output voltage Low High			0.45 V_{CC}	V
I_{LI}	Input current $V_{IN} = 0$ to 5.25V			10	μA
I_{LOH} I_{LOL}	I/O leakage current $\overline{CE} = 2.2\text{V}$ $V_{I/O} = 4.0\text{V}$ $V_{I/O} = 0.45\text{V}$			15 -50	μA
I_{CC1} I_{CC2}	Supply current $V_{IN} = 5.25\text{V}$, $I_{I/O} = 0\text{mA}$ $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$		30	60 70	mA
C_{IN} $C_{I/O}$	Capacitance ³ Input (All pins) I/O $T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$ $V_{IN} = 0\text{V}$ $V_{I/O} = 0\text{V}$		4 10	8 15	pF

AC ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$ unless otherwise specified,
 t_R and $t_F = 20\text{ns}$, $V_{IN} = 0.65\text{V}$ to 2.2V , Timing reference = 1.5V ,
Load = 1 TTL gate and $C_L = 100\text{pF}$

PARAMETER	TO	FROM	2112			2112-1			2112-2			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{RC} t_A t_{CO} t_{CD} t_{OH}	Output Output disable	Chip enable Chip enable	1000 0 40		1000 800 200	500 0 40		500 150 100	650 0 40		650 500 150	ns ns ns ns ns
t_{WC1}	Write cycle		850			500			500			ns
t_{AW1} t_{DW1} t_{CS1} t_{CH1} t_{DH1} t_{CW1}	Setup and hold time Setup time Setup time Hold time Hold time Setup time	Write R/W high CE low CE high Data R/W high	150 650 0 0 100 650		100 250 0 0 50 250			100 280 0 0 50 350				ns
t_{WP1} t_{WR1}	Write pulse width Write recovery time		650 50			250 50			350 50			ns ns
t_{WC2}	Write cycle		1050			500			650			ns
t_{AW2} t_{DW2} t_{CS2} t_{CH2} t_{DH2}	Setup and hold time Setup time Setup time Hold time Hold time	Write R/W high CE low CE high Data	150 650 0 0 100		100 250 0 0 50			100 280 0 0 50				ns
t_{WD2} t_{WR2}	Disable time Write recovery time	R/W high Data	200 50			200 50			200 50			ns ns

NOTES on following page.

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Typical values are for $T_A = 25^\circ\text{C}$ and typical supply voltage.
3. This parameter is periodically sampled and is not 100% tested.

4. Output is enabled and t_{CO} commences only with both CE low and WE high.
5. Output is disabled and t_{DF} combined from either the rising edge of CE or the falling edge of WE.
6. Minimum t_{WP} is valid when CE has been high at least t_{DF} before WE goes low. Otherwise $t_{WP(\min)} = t_{DW(\min)} + t_{DF(\max)}$.
7. When WE goes high at the end of the write cycle, it will be possible to turn on the output buffers if CE is still low. The data out will be the same as the data just written and so will not conflict with input data that may still be on the I/O bus.

VOLTAGE WAVEFORMS

