

1024 BIT READ/WRITE STATIC MOS RAM (1024X1) 21L02/21L02-1/21L02-2/21L02-3

21L02-F,I,N • 21L02-1-F,I,N • 21L02-2-F,I,N • 21L02-3-F,I,N

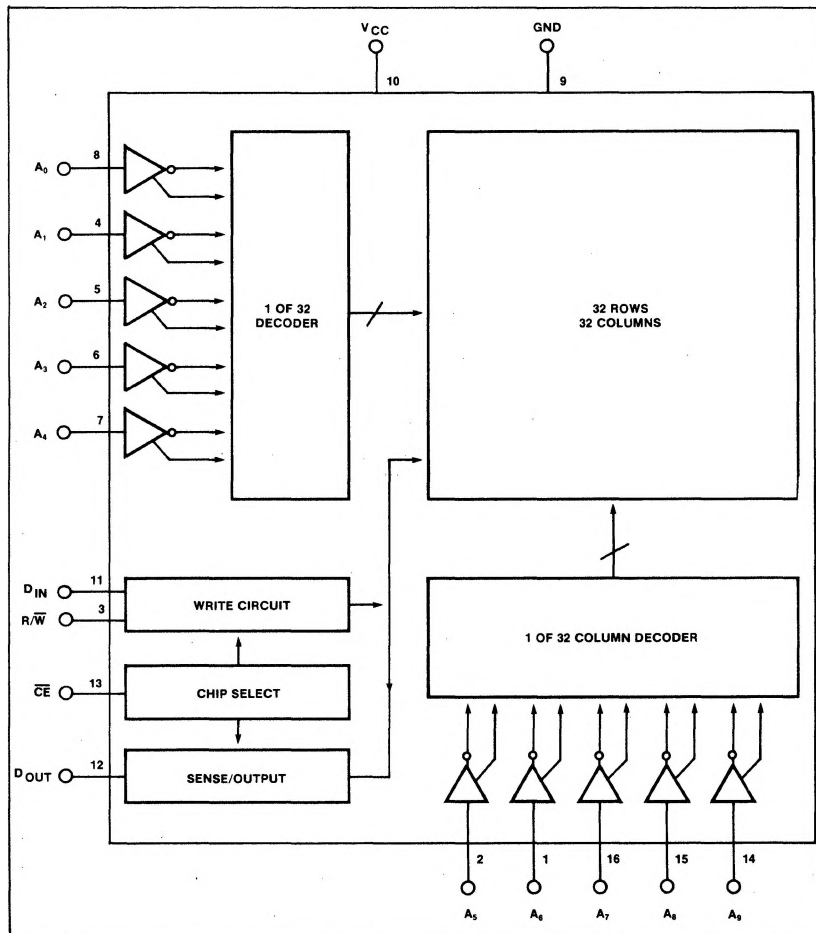
DESCRIPTION

The 21L02, 21L02-1, 21L02-2, and 21L02-3 are low power static random access read/write memories fabricated with low threshold n-channel silicon gate technology.

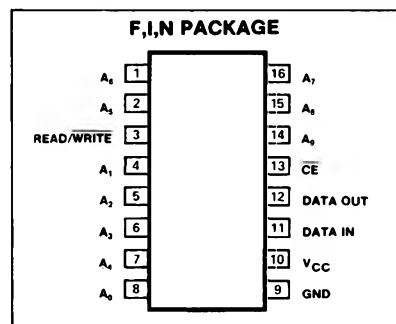
FEATURES

- Fully static
- Requires no clocks
- Completely DTL/TTL compatible
- Single 5V power supply
- Three-state output for OR-tie capability

BLOCK DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS¹

PARAMETER	RATING	UNIT
T _{STG} Temperature range	-65 to 150	°C
P _D Power dissipation ²		
N package	640	mW
F package	1	W
I package	1	W
All input, output and supply voltages with respect to ground	-0.5 to 7	V

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DC ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ ³	Max	
V_{IL} V_{IH}	Input voltage Low High	-0.5 2.2		0.65 V_{CC}	V
V_{OL} V_{OH}	Output voltage Low High			0.45	V
I_{LI}	Input load current (All input pins)	$V_{IN} = 0$ to 5.25V			10 μA
I_{LOH} I_{LOL}	Output leakage current	$\overline{OE} = 2.2\text{V}$ $V_{OUT} = 4.0\text{V}$ $V_{OUT} = 0.45\text{V}$			10 -100 μA
I_{CC1} I_{CC2}	Supply current	All inputs = 5.25V , Data out open $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$			30 40 40 mA

AC ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$ unless otherwise specified, Input pulse levels = 0.65V to 2.2V , Input pulse rise and fall times = 20ns , Timing measurement reference level = 1.5V , Output load = 1 TTL gate and $C_L = 100\text{pF}$

PARAMETER	TO	FROM	21L02			21L02-1			21L02-2			21L02-3			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{RC} t_A t_{CO}	Read cycle Access time		1,000			500			650			400			ns
		Output time			1,000			500			650			400	ns
		Chip enable			500			350			400			300	ns
t_{OH1} t_{OH2}	Previous read data valid with respect to Address Chip enable		50 0			50 0			50 0			50 0			ns
t_{WC} t_{WP} t_{WR}	Write cycle Write pulse width Write recovery time		1,000 750 50			500 300 50			650 400 50			400 250 50			ns ns ns
t_{AW} t_{DW} t_{DH} t_{CW}	Setup and hold time Setup time Setup time Hold time Setup time	Write Rise of $R/\overline{W}$ Change of data in Write	200 800 100 900			150 330 100 400			200 450 100 550			100 300 50 300			ns

NOTES

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device of these or any other condition above those indicated in the operation sections of this specification is not implied.
- For operating at elevated temperatures the device must be derated based on $+150^\circ\text{C}$ maximum junction temperature and a thermal resistance of 150°C/W junction to ambient (B package).
- Typical values are at $+25^\circ\text{C}$ and typical supply voltages.
- All inputs protected against static charge.
- Parameter valid over operating temperature range unless otherwise specified.
- All voltage measurements are referenced to ground.
- Manufacturer reserves the right to make design and process changes and improvements.

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TIMING DIAGRAMS

