

1024-BIT MULTIPLEXED DYNAMIC SHIFT REGISTER (256X4)
1024-BIT MULTIPLEXED DYNAMIC SHIFT REGISTER (512X2)
1024-BIT MULTIPLEXED DYNAMIC SHIFT REGISTER (1024X1)

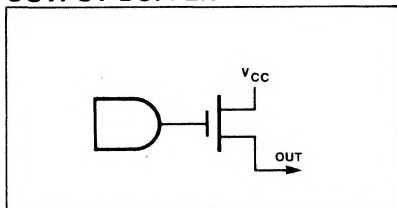
2502
2503
2504

2502-N • 2503-TA,N • 2504-TA,N

DESCRIPTION

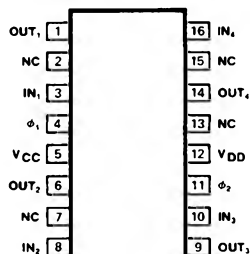
These 2500 Series 1024-bit multiplexed dynamic shift registers consist of enhancement mode p-channel MOS devices integrated on a single monolithic chip. Due to on-chip multiplexing, the data rate is twice the clock rate.

OUTPUT BUFFER

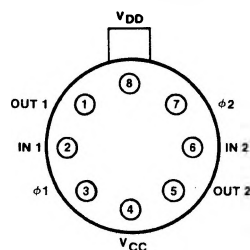


PIN CONFIGURATIONS

**2502
N PACKAGE**



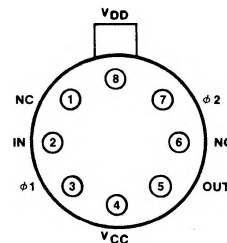
**2503
TA PACKAGE**



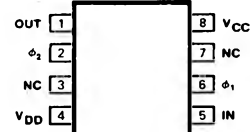
**2503
N PACKAGE**



**2504
TA PACKAGE**



**2504
N PACKAGE**



ABSOLUTE MAXIMUM RATINGS¹

PARAMETER		RATING	UNIT
T _A	Temperature range ²		°C
	Operating	0 to 70	
T _{STG}	Storage	-65 to 150	
P _D	Power dissipation T _A = 70°C ²		mW
	TA and N (8-pin) package	535	
	N (16-pin) package	640	
	Data and clock input voltages and supply voltages with respect to V _{CC} ³	0.3 to -20	V

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2502-N • 2503-TA,N • 2504-TA,N

DC ELECTRICAL CHARACTERISTICS

$T_A = 0^{\circ}\text{C}$ to 70°C , $V_{DD} = -5\text{V} \pm 5\%$, $V_{CC} = 5\text{V}^4$ unless otherwise specified^{5,6,7,8}

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL} V_{IH} V_{ILC} V_{IHC}	Input voltage					V
	Low				1.05	
	High		3.2		5.3	
	Clock low		-10		-12	
V_{OL} V_{OH1} V_{OH2}	Output voltage					V
	Low	$R_L = 3\text{K}$, depends on R_L and TTL gate		-0.3		
	High, driving MOS	$R_L = 5.6\text{K}$	3.6	4.0		
	High, driving TTL	$R_L = 3\text{K}$	3.0	3.5		
I_{LI}	Input load current	$V_{IN} = V_{CC}$ to V_{DD} , $T_A = 25^{\circ}\text{C}$			500	nA
I_{LO} I_{LC}	Leakage current	$T_A = 25^{\circ}\text{C}$				nA
	Output	$V_{\phi 1} = V_{\phi 2} = -10\text{V}$, $V_{OUT} = 0.0\text{V}$		10	1000	
	Clock	$V_{ILC} = -10\text{V}$		10	1000	
I_{DD}	Supply current	Outputs at logic low, 4MHz data rate, $\phi 1 = \phi 2 = 85\text{ns}$ continuous operation, $V_{ILC} = -12\text{V}$, $T_A = 25^{\circ}\text{C}$		15	25	mA
C_{IN} C_{OUT} C_{ϕ}	Capacitance	At 1MHz, 25mV p-p, $T_A = 25^{\circ}\text{C}$				pF
	Input		2.5		5	
	Output		2.5		5	
	Clock		110		150	

AC ELECTRICAL CHARACTERISTICS

$T_A = 25^{\circ}\text{C}$, $V_{DD} = -5\text{V} \pm 5\%$,

$V_{CC} = 5\text{V}^3$, $V_{ILC} = -11\text{V}^{4,5,6,7}$

PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
Freq.	Rep rate				MHz
	Clock	0.0005		4	
	Data	0.001		8	
ϕ_{pw}	Clock pulse width	85			ns
ϕ_D	Clock pulse delay	10			ns
$t_{R,TF}$	Clock pulse transition	10		1000	ns
t_w	Data write time (setup)	50			ns
t_{DO}	Data in overlap	10			ns
t_{A+}, t_{A-}	Data out			90	ns

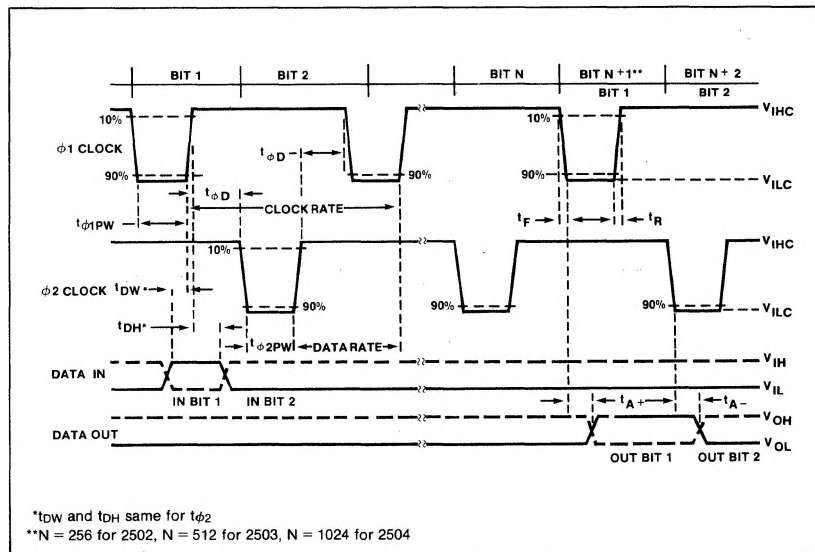
NOTES

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
- For operating at elevated temperatures the device must be derated based on a $+150^{\circ}\text{C}$ maximum junction temperature and a thermal resistance of 150°C/W (TA and V package) or 125°C/W (B package).
- All inputs are protected against static charge.
- V_{CC} tolerance is $\pm 5\%$. Any variation in actual V_{CC} will be tracked directly by V_{IL} , V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.
- Parameters are valid over operating temperature range unless specified.
- All voltage measurements are referenced to ground.
- Manufacturer reserving the right to make design and process changes and improvements.
- Typical values are at $+25^{\circ}\text{C}$ and typical supply voltages.

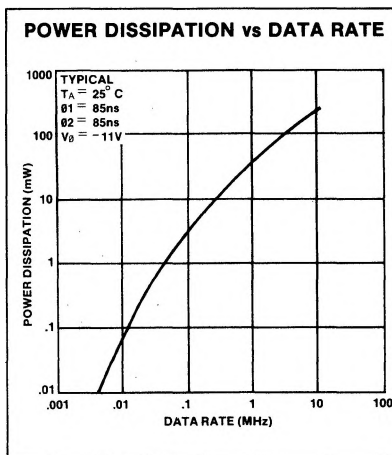
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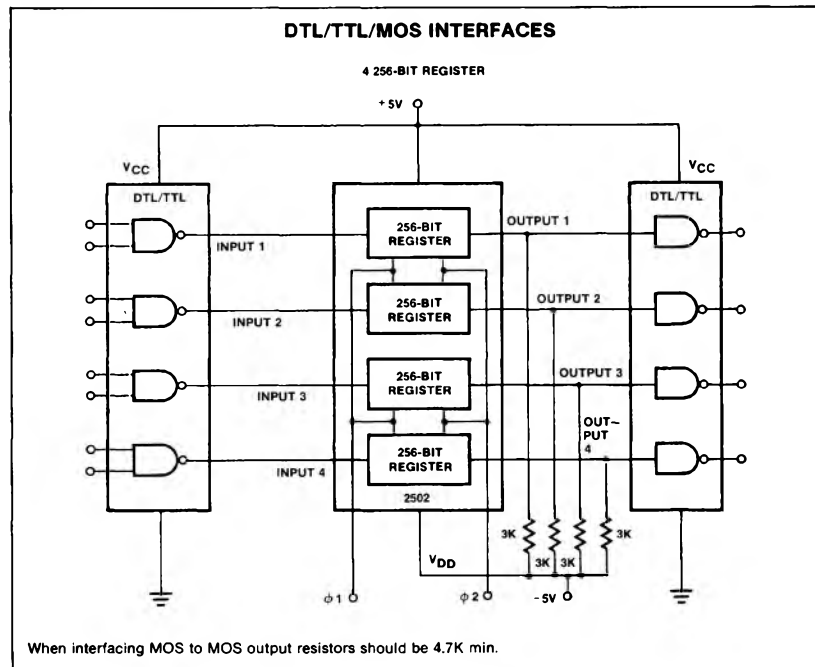
TIMING DIAGRAM



TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL APPLICATIONS



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TYPICAL APPLICATIONS (Cont'd)

