signetics

DUAL 100-BIT DYNAMIC SHIFT REGISTER

SILICON GATE MOS 2500 SERIES

2506
2507
2517

DESCRIPTION

These Signetics 2500 Series dual 100-Bit dynamic shift registers consist of enhancement mode P-channel MOS devices integrated on a single monolithic chip. They use two clock phases.

FEATURES

- HIGH FREQUENCY OPERATION
  4 MHz TYPICAL CLOCK RATE
- TTL, DTL COMPATIBLE
- LOW POWER DISSIPATION — 400 μW/BIT AT 1 MHz
- LOW CLOCK CAPACITANCE 40pF MAXIMUM
- LOW OUTPUT IMPEDANCE — 300 OHMS TYPICAL
- BARE DRAIN AND MOS RESISTOR VERSIONS AVAILABLE
- STANDARD PACKAGES — 8 LEAD TO-5 AND 8 LEAD SILICONE DIP
- SIGNETICS P-MOS SILICON GATE AND SILICONE PACKAGING TECHNOLOGIES

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST BUFFER MEMORIES

PROCESS TECHNOLOGY

Use of the low threshold silicon gate technology allows high speed (3 MHz guaranteed), while reducing power dissipation by a factor of 2 and reducing clock input capacitance dramatically as compared to conventional MOS technologies.

SILICONE PACKAGING

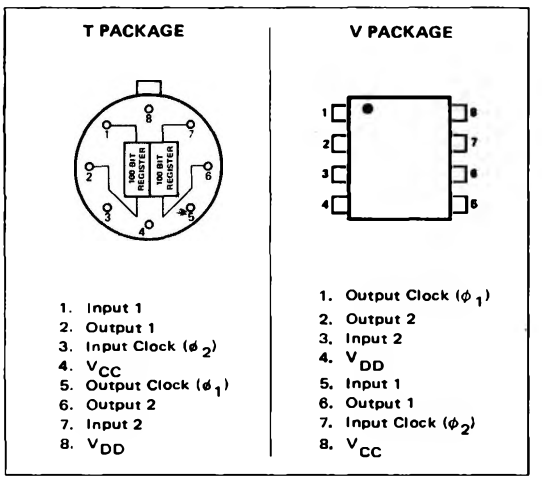
Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric material over the silicon gate-oxide-substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability, demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers. For further information reference Signetics - "Silicone Package Qualification Report".

BIPOLAR COMPATIBILITY

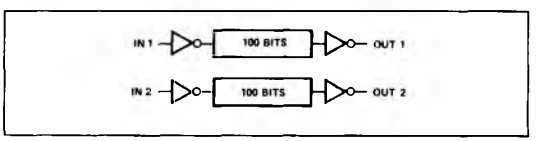
The dual 100 bit device can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.) or by MOS circuits. The design of the output stage provides driving capability for MOS or bipolar IC's.

It is available in bare drain configuration or with internal pull down resistor values of 7.5k or 20k to provide easier interfacing with other MOS circuitry.

PIN CONFIGURATIONS (TOP VIEW)



BLOCK DIAGRAM



PART IDENTIFICATION TABLE

PART NO.	OUTPUT	PACKAGE
2506 T	Bare Drain	8 Pin TO-5
2506 V	Bare Drain	8 Pin DIP
2507 T	7.5k Pull Down	8 Pin TO-5
2507 V	7.5k Pull Down	8 Pin DIP
2517 T	20k Pull Down	8 Pin TO-5
2517 V	20k Pull Down	8 Pin DIP

MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient	0°C + 70°C
Storage Temperature	-65°C + 150°C
Power Dissipation (Note 2) @ T_A=70°C	
T Package	535mW
V Package	455mW
Clock Input Voltages with respect to V_{CC}(3)	+0.3 to -20V
Supply and Data Input Voltages with respect to V_{CC}(3)	+0.3 to -12V

NOTES:
1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W (T package) or 175° C/W (V package).
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.
9. V_{OL} (for this bare drain device) is a function only of the driven gate characteristics together with the external pull-down resistor. (R_{PD}).
10. See Figure 2 for definitions.
11. Logic Convention: Data Lines - Positive; Clocks - Negative.

DC CHARACTERISTICS

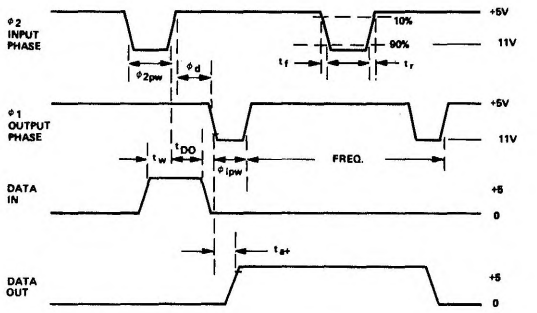
T_A = 0°C to +70°C; V_{DD} = -5V ±5%; V_{CC} = +5 (8); unless otherwise noted(Notes: 4,5,6,7).

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	Input Load Current (Input 1)		10	500	nA	+5V ON OUT 1, ϕ1, ϕ2, V_{CC}, IN 2, OUT 2, IN 1 = −5.5V, V_{DD} = −4.5V, T_A = 25°C
I_{LI}	Input Load Current (Input 2)		10	500	nA	+5V ON OUT 2, ϕ1, ϕ2, V_{CC}, IN 1, OUT 1, IN 2 = −5.5V, V_{DD} = −4.5V, T_A = 25°C
I_{LO}	Output Leakage Current (OUT 1) (Notes 9 & 10)		10	1000	nA	+5V ON IN 1, V_{CC}, OUT 2, ϕ2, IN 2, V_{DD}, OUT 1 = −5.5V ϕ1 = −10V, T_A = 25°C (2506 Only)
I_{LO}	Output Leakage Current (OUT 2) (Notes 9 & 10)		10	1000	nA	+5V ON IN 1, OUT 1, V_{CC}, ϕ2, IN 2, V_{DD}, OUT 2 = −5.5V, ϕ = −10V, T_A = 25°C (2506 Only)
I_{LC}	Clock Leakage Current (ϕ1)		10	1000	nA	Vϕ1 = −12 V, V_{DD} = −4.5V All other pins +5V, T_A = 25°C
I_{LC}	Clock Leakage Current (ϕ2)		10	1000	nA	Vϕ2 = −12 V, V_{DD} = −4.5V All other pins +5V T_A = 25°C
V_{IL}	Input "Low" Voltage (Note 11)	−5		1.05	V	
V_{IH}	Input "High" Voltage (Note 11)	3.2		5.3	V	
C_{IN}	Input Capacitance (Inputs 1 & 2)		2.5	5	pF	V_{IN} = V_{CC}, 1 MHz, 25 mV p-p
C_{ϕ}	Clock Input Capacitance (ϕ1, ϕ2)		25	40	pF	V_{ϕ} = V_{CC} , 1 MHz, 2 5 mV p-p
V_{IHC}	Clock Input "High" Voltage	4		5.3	V	
V_{ILC}	Clock Input "Low" Voltage	−12		−10	V	

CONDITIONS OF TEST

Data amplitude +1.05 to +3.2 Input rise and fall times: 10 nsec. Output load is 1 TTL gate.

TIMING DIAGRAM



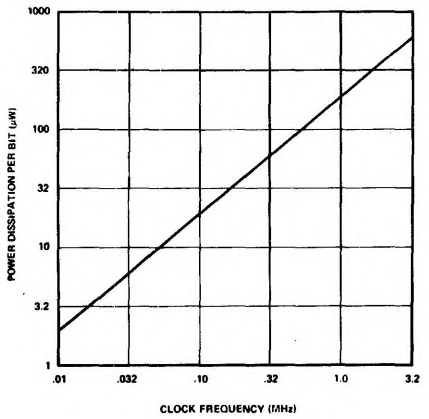
AC CHARACTERISTICS

$T_A = 25°C$; $V_{DD} = -5V \pm 5\%$; $V_{CC} = +5V$ (8) ; $V_{ILC} = -11V$

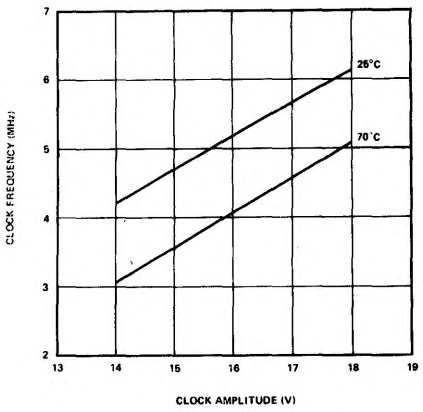
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
Frequency	Clock Rep Rate	0006	4	3	MHz	
ϕ IPW	Clock Pulse Width ϕ 1	150			nsec	@ 3MHz.
ϕ 2PW	Clock Pulse Width ϕ 2	100			nsec	@ 3MHz.
ϕ_d	Clock Pulse Delay	10			nsec	@ 3MHz
t_r, t_f	Clock Pulse Transition	10		1000	nsec	
t_W	Data Write Time (Set-Up)	75				
t_{DO}	Data In Overlap	10				$t_{r\phi 2} = t_{r\phi 1} = 10nS$
t_{a+}	Clock to Data Out		90	150		V ϕ = V_{CC} - 16V, DATA OUT =+2.5V
V_{OH1}	Output "High" Voltage driving MOS (Note 11)	3.4	4.0		V	R_{INT} = 7.5k nom., C_L = 10pF, 2507 Only, R_{INT} = 20k nom. 2517 only
V_{OH2}	Output "High" Voltage driving TTL (Note 11)	3.0	3.5		V	R_L = 3.3k, V_{DD} = -5V 2506 only
I_{DD}	Power Supply Current (V_{DD})		12	26	mA	Outputs @ logic "0" or "1", 3MHz, ϕ 1 = 150ns, ϕ 2 = 100ns

CHARACTERISTIC CURVES

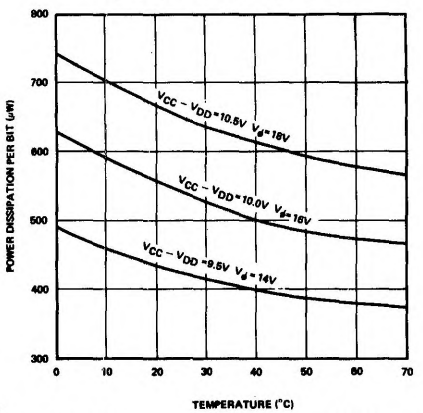
POWER DISSIPATION PER BIT VERSUS FREQUENCY



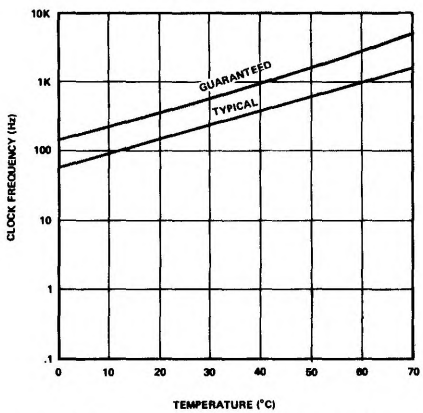
TYPICAL CLOCK FREQUENCY VERSUS CLOCK AMPLITUDE



POWER DISSIPATION BIT VERSUS TEMPERATURE



MINIMUM OPERATING CLOCK RATE

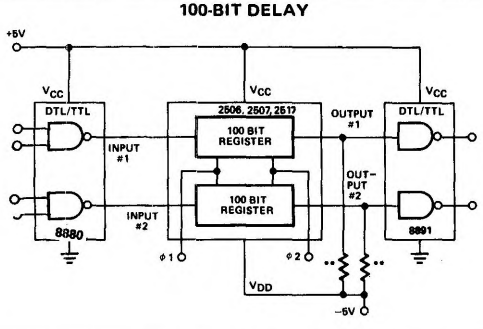


NOTE:
Contitions for Typical Curves: V_{CC}=+5V, V_{DD}=-5V. V_{ILC}=-11V, ϕ_{PW1}=150ns, ϕ_{PW2}=100ns, f=3MHz, T_A=+25°C unless otherwise noted.

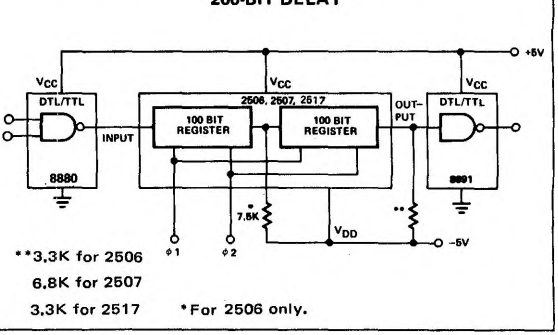
APPLICATIONS DATA

DTL/TTL/MOS INTERFACES

100-BIT DELAY



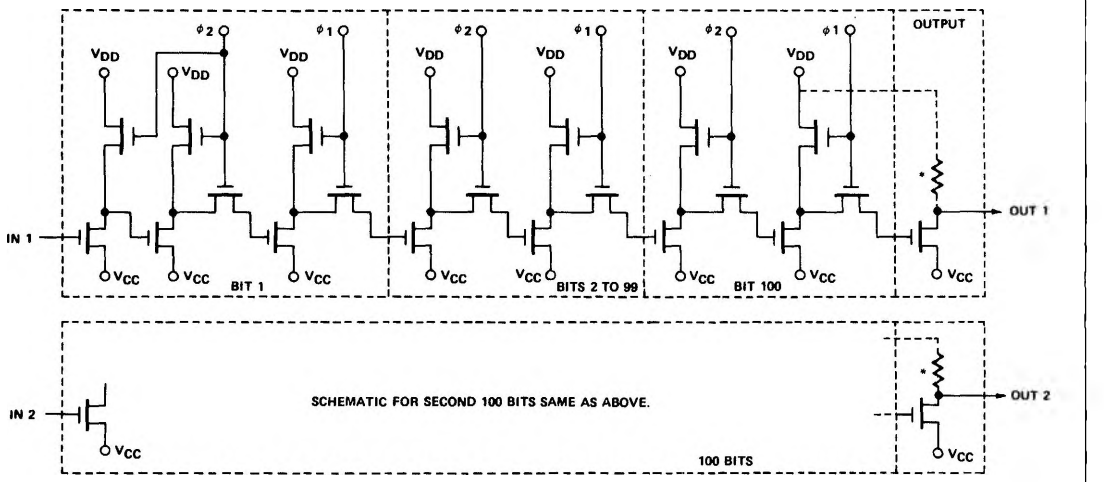
200-BIT DELAY



**3.3K for 2506
6.8K for 2507
3.3K for 2517

*For 2506 only.

CIRCUIT SCHEMATIC



*For 2507 and 2517 Options Only.