DUAL 50-BIT STATIC SHIFT REGISTER (50X2) 2509
DUAL 100-BIT STATIC SHIFT REGISTER (100X2) 2510
DUAL 200-BIT STATIC SHIFT REGISTER (200X2) 2511

2509-N,K • 2510-N,K • 2511-N,K

DESCRIPTION

The 2509 50-bit, 2510 100-bit, and the 2511 200-bit recirculating static shift registers consist of enhancement mode p-channel silicon gate MOS devices integrated on a single monolithic chip. Internal recirculation logic plus TTL/DTL level clock signals plus tri-state outputs are provided for maximum interfacing ease.

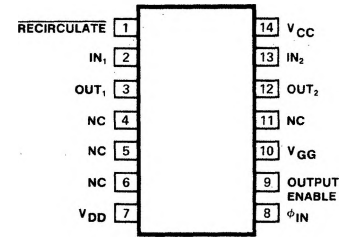
TRUTH TABLE

RECIRCULATE	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is written
1	1	"1" is written

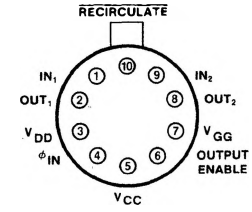
"0" = OV; "1" = +5V.

PIN CONFIGURATIONS

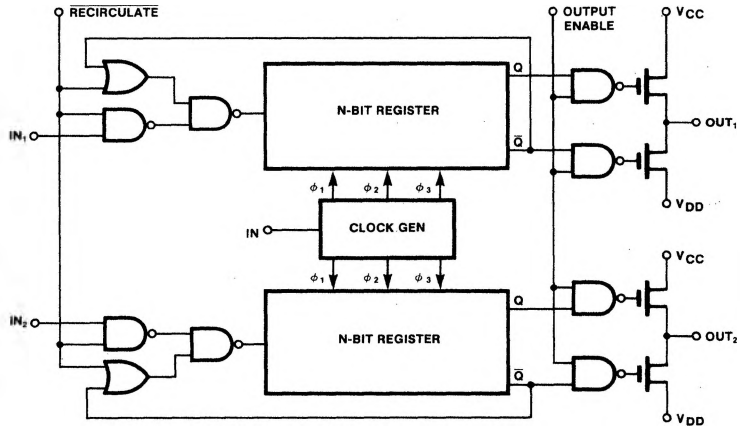
N PACKAGE



K PACKAGE



BLOCK DIAGRAM



NOTES

A. N = 50 for 2509, N = 100 for 2510, N = 200 for 2511.
B. If output enable = low, output is off.
C. If output enable = high, see Truth Table.

ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating[2]	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation at T_A = 70°C[2]	535	mW
	Data and clock input voltages and supply voltages with respect to V_{CC}[3]	0.3 to -20	V

2509-N,K • 2510-N,K • 2511-N,K

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V[4], V_{DD} = -5V ± 5%, V_{GG} = -12V ± 5% unless otherwise specified[5,6,7,8]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage[4]					V
V_{IL}	Low				0.6	
V_{IH}	High		3.4		5.3	
V_{ILC}	Clock low		-5		0.6	
V_{IHC}	Clock high		3.4		5.3	
	Output voltage					V
V_{OL}	Low	I_{OL} = 1.6mA			0.5	
V_{OH}	High	I_{OH} = 100μA	3.8	3.5		
	Driving MOS		3.6			
	Leakage current	T_A = 25°C				nA
I_{LO}	Output	V_{CE} = 1.05V, V_{OUT} = -5V		10	1000	
I_{LC}	Clock	V_{ILC} = GND		10	500	
I_{DD}	Supply current	Continuous operation, T_A = 25°C, f = 1.5MHz				mA
	Dual 50			6.5	15	
	Dual 100			12	30	
	Dual 200			20	40	
I_{GG}				4.5	7.5	
I_{LI}	Input load current	V_{IN} = -5.5V, T_A = 25°C		10	500	nA
	Capacitance	At 1MHz; V_{AC} = 25mV p-p				pF
C_{IN}	Input	$V_{IN} = V_{CC}$			5	
C_{OUT}	Output	$V_{OUT} = V_{CC}$			5	
C_{ϕ}	Clock	$V_{\phi} = V_{CC}$			5	

AC ELECTRICAL CHARACTERISTICS

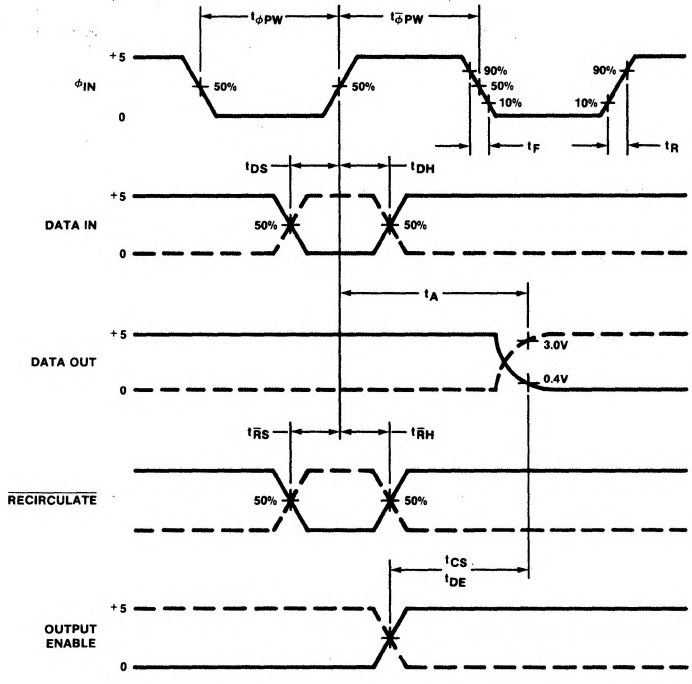
V_{CC} = 5V[4], V_{DD} = -5V ± 5%, V_{ILC} = 0.4V to 4V, V_{GG} = -12V ± 5%, T_A = 0°C to 70°C.

PARAMETER		TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
Freq.	Clock rep rate				dc	3	1.5	MHz
	Pulse width							μs
$t_{\phi}PW$	Clock				.290	150	100	
$t_{\overline{\phi}}PW$	$\overline{\text{Clock}}$				.210		dc	
	Setup and hold time							ns
t_{DS}	Setup time	ϕin	Data in		50			
t_{DH}	Hold time	Data in	ϕin		70			
	Propagation delay							ns
t_A		Data out	Clock			200	350	
t_A				I_{OL} = 1.6mA			500	
T_{CS}	Select time	Data out	Output enable				300	ns
T_{DE}	Deselect time						300	ns
t_R,t_F	Clock pulse transition						1	μs

NOTES

1. Stresses above those listed under absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 150°C/W.
3. All inputs are protected against static charge accumulation.
4. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to 70°C. Actual input requirements with respect to V_{CC} are $V_{IH} = V_{CC}$ -1.85V and $V_{IL} = V_{CC}$ -4.15V.
5. Parameters are valid over operating temperature range unless otherwise specified.
6. All voltage measurements are referenced to ground.
7. Manufacturer reserves the right to make design and process changes and improvements.
8. Typical values are at 25°C and typical supply voltages.

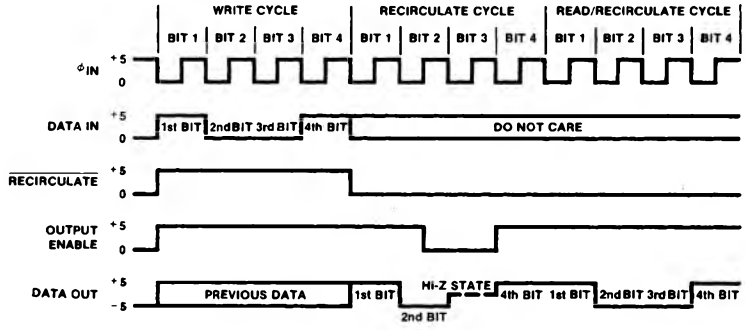
TIMING DIAGRAM



$t_R = t_F < 10ns$ for all inputs

TYPICAL APPLICATION

EXAMPLE FOR 4-BIT SHIFT REGISTER



NOTES

A. Write Cycle: The positive going edge of the recirculate control is coincident with the negative-going clock edge. The output enable control may be either high or low. If it is high, previous data will be read, and the 1st bit will be read after the fourth rising clock edge.

B. Recirculate Cycle: Data Recirculates while the recirculate control is low. Output enable may be either high or low. If it is low, the output is in the high impedance state.

C. Read/Recirculate Cycle: Data is read out while the output enable is high. Data is also recirculated as long as the recirculate control is low.