2524-N • 2525-N

DESCRIPTION

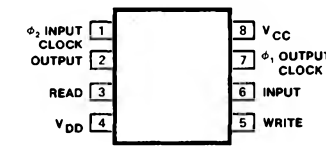
The 2525 1024-bit recirculating dynamic shift register consists of enhancement mode p-channel MOS devices integrated on a single monolithic chip. Internal recirculation logic plus write and read controls are included on the chip.

TRUTH TABLE

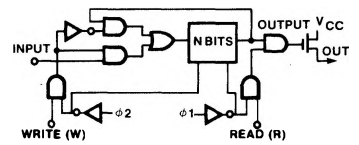
WRITE	READ	FUNCTION
0	0	Recirculate, Output is '0'
0	1	Recirculate, Output is data
1	0	Write mode, Output is '0'
1	1	Read mode, Output is data

PIN CONFIGURATION

N PACKAGE



BLOCK DIAGRAM



N = 512 or 1024, Low = 0V, High = +5V

ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range[2]		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation at $T_A > 70°C$[2]	535	mW
	Data and clock input voltages and supply voltages with respect to V_{CC}	0.3 to -20	V

DC ELECTRICAL CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = -5V \pm 5\%$ unless otherwise specified.

	PARAMETER	TEST CONDITIONS	2524			2525			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Input voltage[3]								V
V_{IL}	Low		-5.0		0.6	-5.0		0.6	
V_{IH}	High		3.4		5.3	3.4		5.3	
V_{ILC}	Clock low		-12.0		-10.0	-12.0		-10.0	
V_{IHC}	Clock high		4.0		5.3	4.0		5.3	
	Output voltage								V
V_{OL}	Low, driving 1 TTL load	$R_L = 3.0K$, 1 TTL load ($I_L = 1.6mA$)[4]		-1.0			-1.0		
V_{OH1}	High, driving 1 TTL load	$R_L = 3.0K$, 1 TTL load ($I_L = 100\mu A$)	2.4	3.5		2.4	3.5		
V_{OH2}	High, driving MOS	$R_L = 5.6K$, $C_L = 10pF$	3.6	4.0		3.6	4.0		
I_{LI}	Input load current	$V_{IN} = -5.5V$, $T_A = 25°C$		10	500		10	500	nA
	Leakage current	$T_A = 25°C$							nA
I_{LO}	Output	$V_{\phi 2} = V_{\phi 1} = -12V$, $V_{DD} = -5$, $V_{OUT} = -5.5V$		10	1000		10	1000	
I_{LC}	Clock	$V_{ILC} = -12V$		10	1000		10	1000	
I_{DD}	Supply current	Continuous operation, $\phi pW = 150ns$, $f = 1MHz$, $V_{ILC} = -12V$, $T_A = 25°C$, $V_{DD} = -5.5V$		15	35		25	35	mA
	Capacitance	1MHz, $V_{AC} = 25mV$ p-p							pF
C_{IN}	Input	$V_I = V_{CC}$			5			5	
C_{OUT}	Output	$V_O = V_{CC}$			5			5	
C_ϕ	Clock	$V = V_{CC}$			80			160	

AC ELECTRICAL CHARACTERISTICS

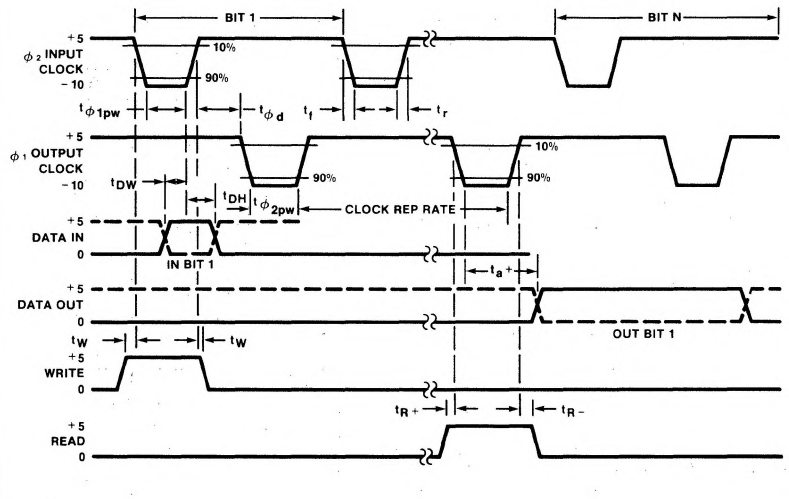
T_A = 25°C, V_{CC} = 5V ± 5%, V_{DD} = -5V ± 5%, V_{ILC} = -11V,
Input rise and fall times = 10ns, Output load = 1 TTL gate

PARAMETER		TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
Freq.	Clock data rep rate[5]			W = R = V_{CC}	.0005	5	3	MHz
$t_{\phi}PW$	Clock pulse width				135	85		ns
$t_{\phi D}$	Clock pulse delay				10			ns
t_R,t_F	Clock pulse transition				10		1000	ns
	Setup and hold time							ns
t_{DW}	Setup time	Clock	Data in		70			
t_{DH}	Hold time	Data in	Clock		20			
t_{A+}	Delay time	Data out	Clock				100	ns
t_{R-},t_{W-}	Clock to read or write timing				0			ns
t_{R-},t_{W+}	Clock to read or write timing				0			ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are $V_{IH} = V_{CC} - 1.85V$ and $V_{IL} = V_{CC} - 4.15V$.
4. V_{OL} is a function of the input characteristics of the driven TTL/DTL gate I_{OI} and V_{CLAMP} and the value of the pull-down resistor (R_L).
5. See Minimum Operating Frequency graph for low limits on data rep. rate.
6. All inputs are protected against static charge.
7. All voltage measurements are referenced to ground.
8. Manufacturer reserving the right to make design and process changes and improvements.
9. Typical values are at +25°C and typical supply voltages.
10. Parameters are valid over operating temperature range unless otherwise specified.

TIMING DIAGRAM



NOTES

A. N = 512 for 2524, N = 1024 for 2525.
B. Note that the read input is AND'ed with $\overline{\phi_1}$; therefore this function is not valid until ϕ_1 occurs.