signetics

1024-BIT STATIC SHIFT REGISTER | 2533

PRELIMINARY SPECIFICATIONS

DESCRIPTION

The Signetics 2533 Static Shift Register consists of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip.

The 1024-bit register is equipped with two data inputs together with a "Stream Select" control to facilitate external recirculation.

The single phase clock input, data input, data output, and stream select control will interface directly with TTL/DTL circuits without external components.

Data is entered when the clock is at a logic "1". Data is shifted when the clock goes low.

FEATURES

- TOTAL TTL COMPATIBILITY
- SINGLE CLOCK LINE
- DC TO 1.5MHz GUARANTEED
- LOW POWER (TYPICALLY 250μW/BIT)
- POWER SUPPLIES +5V AND −12V
- 8-PIN DIP
- STREAM SELECT FOR EASY RECIRCULATION

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST STATIC BUFFER MEMORIES
CRT REFRESH – LINE AND PAGE
DELAY LINES
DRUM MEMORY REPLACEMENT

SPECIAL FEATURES

The three clock phases used in the static register cells are generated internally by an on-chip generator. This clock generator is controlled by a single TTL/DTL 5V logic level input.

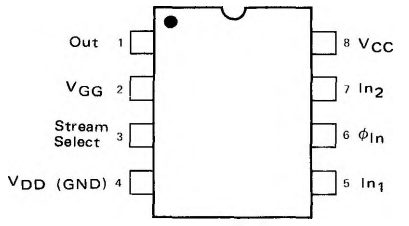
Recirculation of data in the 2533 is accomplished by simply jumpering the output back to In 2. The stream select control then becomes a Data Entry/Recirculate Control.

BIPOLAR COMPATIBILITY

All inputs of this register, including the clock, can be driven directly by bipolar TTL/DTL integrated circuits without external components. Each input is equipped with an internal pull-up resistor to enhance the "1" level of the TTL driver. The output is push-pull, operating between 0V and +5V, and provides a sink current of 1.6mA for one TTL fanout.

PIN CONFIGURATION: (Top View)

"V" PACKAGE

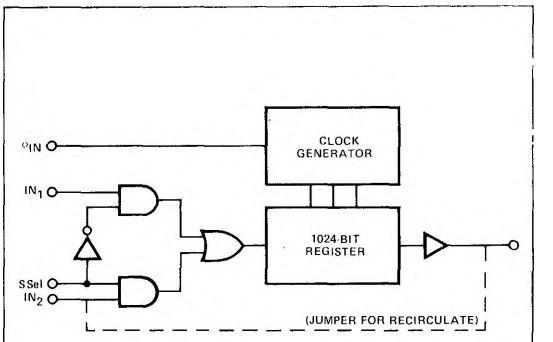


TRUTH TABLE

STREAM SELECT	FUNCTION
0	IN 1
1	IN 2

NOTE: "0" = 0V, "1" = +5V

BLOCK DIAGRAM



PART IDENTIFICATION TABLE

PART NUMBER	BIT LENGTH	PACKAGE
2533 V	1024	8-Pin DIP

MAXIMUM GUARANTEED RATINGS(1)

Operating Ambient Temperature(2)	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation (Note 2)	535mW @ T_A >25°C
Data and Clock Input Voltages and Supply Voltages with Respect to V_{CC}	+0.3V to −20V

DC CHARACTERISTICS

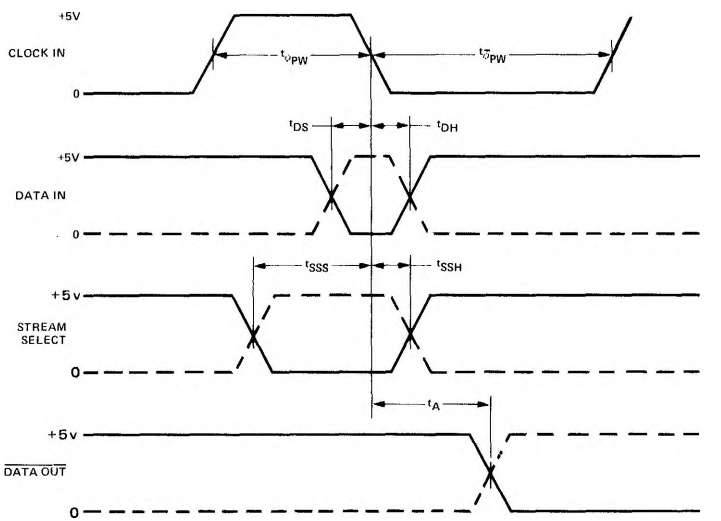
(T_A = 0°C to +70°C; V_{CC} = +5V ±5%; V_{GG} = −12V ±5% unless otherwise noted.)

SYMBOL	TEST	MIN.	TYP.	MAX.	UNITS	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} = 0, T_A = 25°C
I_{LC}	Clock Leakage Current		10	500	nA	V_{ILC} = GND, T_A = 25°C
I_{CC}	Power Supply Current		16	30	mA	Continuous Operation
I_{GG}	Power Supply Current		5.0	7.5	mA	F = 1.5MHz
V_{IL}	Input "Low" Voltage			0.8	V	V_{CC} = +5V
V_{IH}	Input "High" Voltage	3.2			V	V_{CC} = +5V
V_{ILC}	Clock Input "Low" Voltage			0.8	V	V_{CC} = +5V
V_{IHC}	Clock Input "High" Voltage	3.2		5.3	V	V_{CC} = +5V

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated corresponding to a thermal resistance of 150°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.

TIMING DIAGRAM

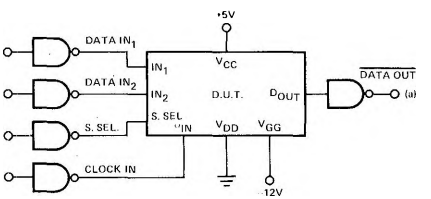


NOTE: Times measured at 50% points with input tr, tf ≤ 10ns.

AC CHARACTERISTICS V_{CC} = +5V ± 5%; V_{GG} = -12V ± 5%; T_A = 0° to +70°C

SYMBOL	TEST	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Frequency	Clock & Data Rep Rate	DC	2	1.5	MHz	
$t_{\phi PW}$	Clock Pulse Width	.350		100	μs	
$t_{\bar{\phi} PW}$	Clock Pulse Width	250		DC	ns	
t_r, t_f	Clock Pulse Transition			1	μs	
t_{DS}	Data Write Set-Up Time	50			ns	
t_{DH}	Data to Clock Hold Time	50			ns	
t_A	Clock to Data Out Delay		200	400	ns	I_{OL} = 1.6mA
t_{SSH}	Stream Select Hold Time	50			ns	
t_{SSS}	Stream Select Set-Up Time	80			ns	
C_{IN}	Input Capacitance			5	pF	@ 1 MHz, V_{IN} = V_{CC} V_{AC} = 25mV p-p
C_{OUT}	Output Capacitance			5	pF	@ 1 MHz, V_{OUT} = V_{CC} V_{AC} = 25mV p-p
C_ϕ	Clock Capacitance			5	pF	@ 1 MHz, V_ϕ = V_{CC} V_{AC} = 25mV p-p
V_{OL}	Output "Low" Voltage			0.4	V	1 TTL load (I=1.6mA)
V_{OH}	Output "High" Voltage	2.4	3.5		V	1 TTL load (I=-100μA)

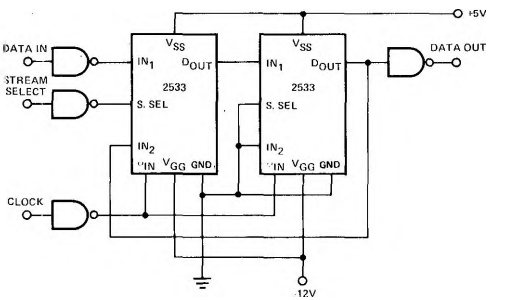
A.C. TEST SETUP



NOTES:
Measure T_Λ between device input and point (a).
Gates are standard 8800 or 7400.

APPLICATIONS INFORMATION

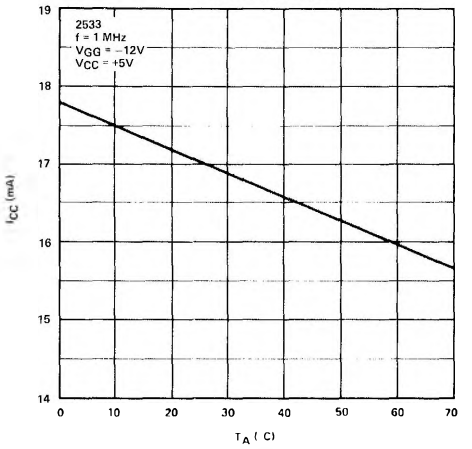
2048-BIT STORAGE REGISTER WITH RECIRCULATE



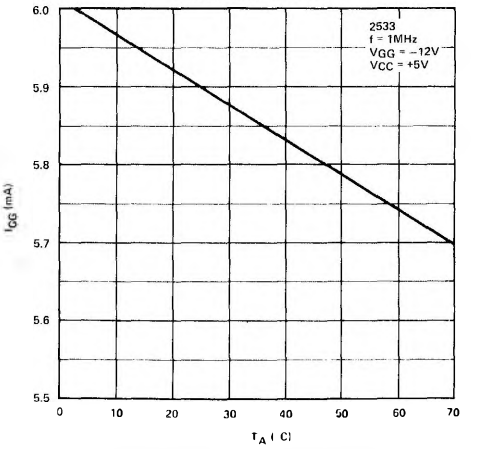
NOTE:
Gates are standard DTL or TTL.

CHARACTERISTIC CURVES

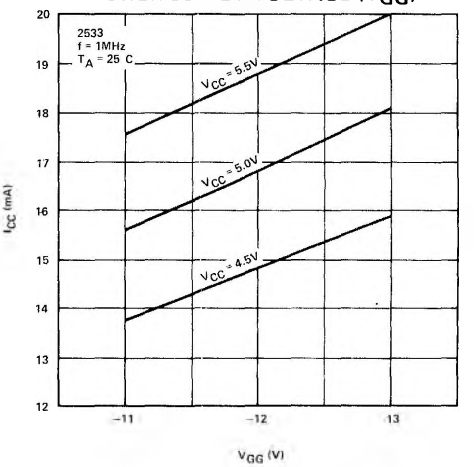
POWER SUPPLY CURRENT (I_{CC}) VERSUS TEMPERATURE



POWER SUPPLY CURRENT (I_{GG}) VERSUS TEMPERATURE



POWER SUPPLY CURRENT (I_{CC}) VERSUS POWER SUPPLY VOLTAGE (V_{GG})



POWER SUPPLY CURRENT (I_{GG}) VERSUS POWER SUPPLY VOLTAGE (V_{GG})