signetics

FULLY DECODED 256×1 STATIC RANDOM ACCESS MEMORY | 25L01

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The Signetics 25L01 256 x 1 Random Access Memory employs enhancement mode P-channel MOS devices integrated on a single monolithic chip. It is fully decoded, permitting the use of a 16-pin dual in-line package. Complete static operation requires no clocking. The 25L01 is optimized with +5 and -12V supplies.

FEATURES

- FULLY DECODED ADDRESS
- ACCESS TIME – 1.0 μs GUARANTEED
- POWER DISSIPATION – 1.7 MW BIT MAXIMUM DURING ACCESS
- STANDBY POWER DISSIPATION – 100 μW/BIT
- DTL AND TTL COMPATIBLE
- CHIP SELECT AND OUTPUT WIRED-OR CAPABILITY FOR EASY EXPANSION
- STANDARD 16-PIN DIP SILICONE OR CERAMIC PACKAGE
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY
- V_{CC} = +5V, V_{DD} = V_D = -12V

APPLICATIONS

SMALL BUFFER STORES
SMALL CORE MEMORY REPLACEMENT
BIPOLAR COMPATIBLE DATA STORAGE

SILICONE PACKAGING

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric material over the silicon gate-oxide-substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability and demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers.

BIPOLAR COMPATIBILITY

All inputs of the 25L01 can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.). The data output buffers are capable of sinking a minimum of 2.0 mA, sufficient to drive one standard TTL load.

POWER DISSIPATION

The maximum power dissipation of 1.7 mW/bit is required only during Read or Write. For standby operation 100 μW/bit is obtained by removing V_D and reducing V_{DD} to –8.0V. Removal of V_D alone will cut power dissipation by a factor of almost 3.

TRI-STATE OUTPUT

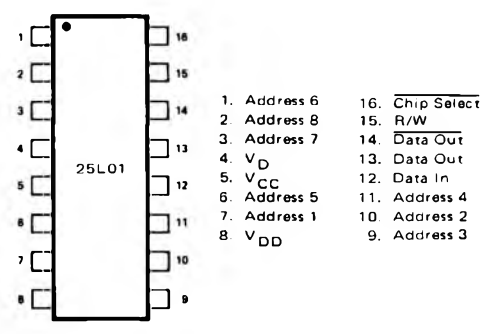
The outputs of the 25L01 are effectively open circuited when the device is not selected (logic 1 on chip select). This feature allows OR-tieing for memory expansion.

PART IDENTIFICATION TABLE

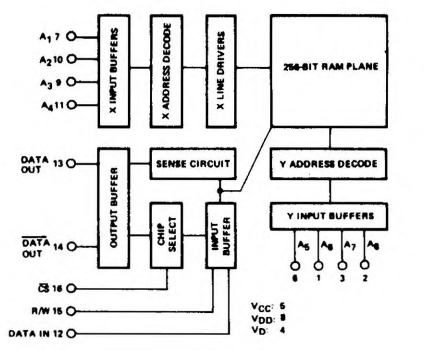
TYPE	PACKAGE	OP. TEMP. RANGE
25L01B	16-pin Silicone DIP	0°C to +70°C
25L01I	16-pin Ceramic DIP	0°C to +70°C

PIN CONFIGURATION (Top View)

B/I PACKAGE



BLOCK DIAGRAM



MAXIMUM GUARANTEED RATINGS (1)

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to the Most Positive Supply Voltage, V_{CC}	+0.3V to -20V
Supply Voltages V_{DD} and V_D with Respect to V_{CC}	-18V
Power Dissipation at T_A = 25°C "B" pkg.	640 mW
"I" pkg.	800 mW

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device of these or any other condition above those indicated in the operation sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient ("B" pkg.) ("I" pkg., 100°C/W).
3. All inputs protected against static charge.
4. Parameter valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.

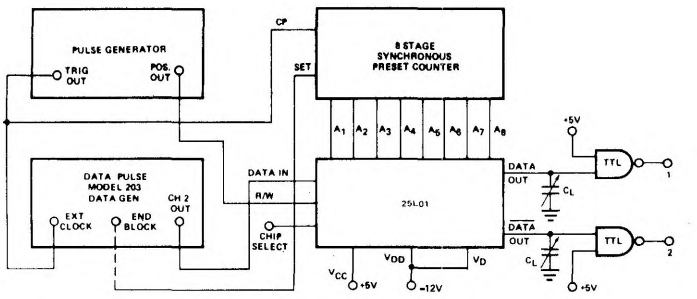
DC CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, V_{DD} = V_D = -12V ± 5% unless otherwise specified. See notes above).

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	Input Load Current (All Input Pins)		<1.0	500	nA	V_{IN} = 0.0V; T_A = +25°C
I_{LO}	Output Leakage Current		<1.0	1000	nA	V_{OUT} = 0.0V, Chip Select Input = +3.3V, T_A = +25°C
I_{DD}	Power Supply Current, V_{DD}		5	9	mA	T_A = +25°C
I_D	Power Supply Current, V_D		11	16	mA	I_{OL} = 0.0 mA T_A = +25°C
V_{IL}	Input "Low" Voltage	−12		V_{CC}−4.5	V	
V_{IH}	Input "High" Voltage	V_{CC}−2.0		V_{CC}+0.3	V	
I_{OL1}	Output Sink Current	3.0	6		mA	V_{OUT} = +0.45V, T_A = +25°C
I_{OL2}	Output Sink Current	2.0	5		mA	V_{OUT} = +0.45V, T_A = +70°C
I_{OL3}	Output Sink Current		6	13	mA	V_{OUT} = −0.7 V
I_{OH1}	Output Source Current	−3.0	4		mA	V_{OUT} = 0.0V, T_A = +25°C
I_{OH2}	Output Source Current	−2.0	3		mA	V_{OUT} = 0.0V, T_A = +70°C
V_{OL}	Output "Low" Voltage		−0.7	+0.45	V	I_{OL} = 3.0 mA
V_{OH}	Output "High" Voltage	+3.5	+4.5		V	I_{OH} = −100μA
C_{IN}	Input Capacitance (All Input Pins)		7	10	pF	V_{IN} = +5.0V f = 1 MHz
C_{OUT}	Output Capacitance		7	10	pF	V_{OUT} = +5.0 V f = 1 MHz

SWITCHING CHARACTERISTICS Guaranteed Limits T_A = 0 to +70°C, V_{CC} = +5V ±5%, V_{DD} = V_D = -12V ±5%

READ CYCLE			WRITE CYCLE		
SYMBOL	TEST	LIMITS (μsec) MAX	SYMBOL	TEST	LIMITS (μsec) MIN.
t_a	Access Time	1 μsec	t_{WD}	Address to Write Pulse Delay	0.3
			t_{WP}	Write Pulse Width	0.4
			t_W	Write Time	0.3
			t_{DO}	Data-Write Pulse Overlap	0.1

TEST SETUP FOR SPEED MEASUREMENT



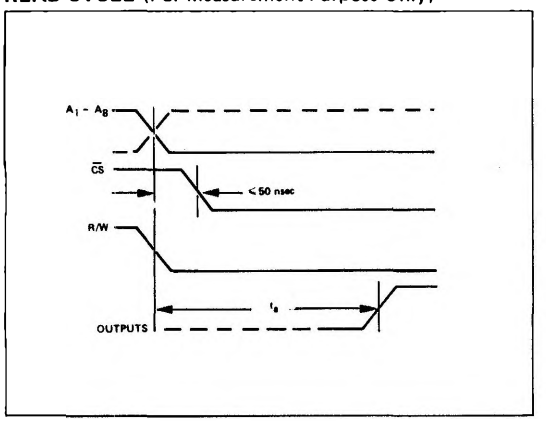
NOTES:

1. Each clock time is split into a Read followed by a Write. Read and Write times can be varied by adjustment of the "delay" and "width" controls of the pulse generator.
2. Data generator produces a 256-bit block of data, 32 bits repeated 8 times. "PCM" mode used so data can be changed in 32 bits of the 25L01 from one cycle to the next.
3. All inputs to the 25L01 are standard TTL outputs with V_{CC} = +5V ±5%.
4. Access time is measured between A1 (least significant address input) and points 1 and 2.

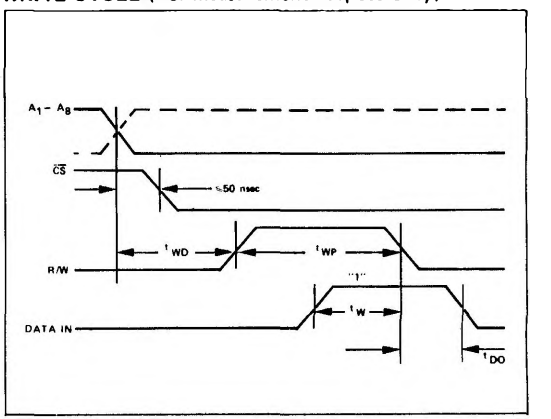
CONDITIONS OF TEST

Input pulse amplitudes: 0 to +5V, Input pulse rise and fall times: < 10 nsec. Speed measurements referenced to 1.5V levels. Output load is 1 TTL gate; measurements made at output of TTL gate ($t_{pd} \leq$ 10 nsec).

READ CYCLE (For Measurement Purpose Only)



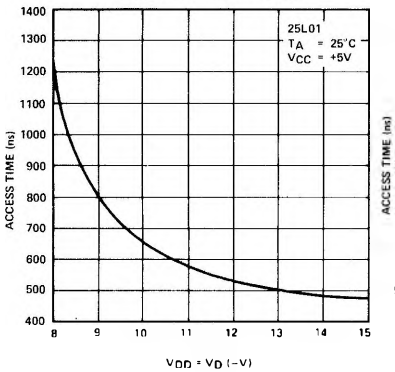
WRITE CYCLE (For Measurement Purpose Only)



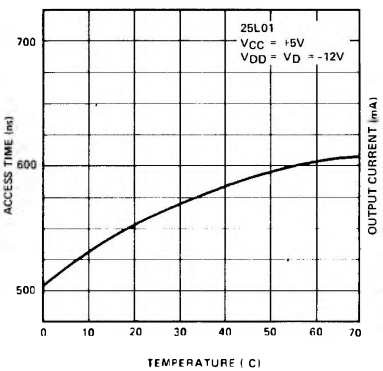
APPLICATION INFORMATION: Reference 2501 specifications.

TYPICAL CHARACTERISTIC CURVES

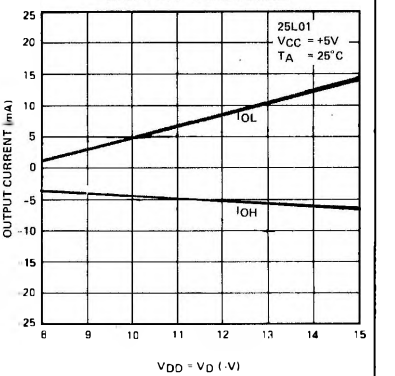
ACCESS TIME VERSUS SUPPLY VOLTAGE



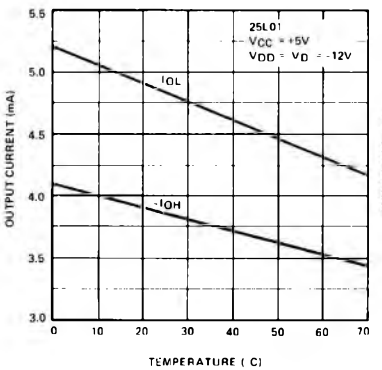
ACCESS TIME VERSUS TEMPERATURE



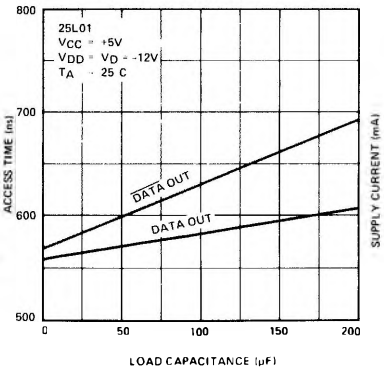
OUTPUT CURRENT VERSUS SUPPLY VOLTAGE



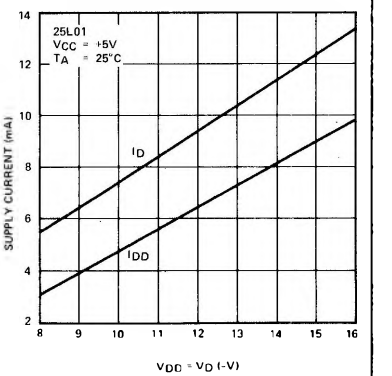
OUTPUT CURRENT VERSUS TEMPERATURE



ACCESS TIME VERSUS LOAD CAPACITANCE



POWER SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



ACCESS TIME VERSUS SUPPLY VOLTAGES