# 4096-BIT ERASABLE AND ELECTRICALLY REPROGRAMMABLE MOS ROM (512X8) 2704
# 8192-BIT ERASABLE AND ELECTRICALLY REPROGRAMMABLE MOS ROM (1024X8) 2708

2704-I • 2708-I

## DESCRIPTION

The 2708/2704 are high speed Erasable and Electrically Reprogrammable ROMs (EPROM) ideally suited where fast turn around and pattern experimentation are important requirements.

The 2708/2704 are packaged in a 24 pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device.

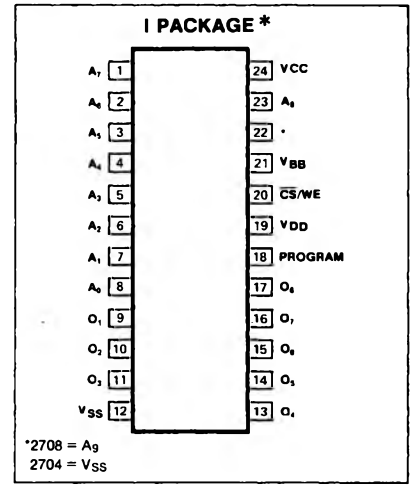
A pin for pin mask programmed ROM, the Signetics 2607, is available for large volume production runs of systems initially using the 2708.

The 2708/2704 is fabricated with the time proven n-channel silicon gate technology.

## FEATURES

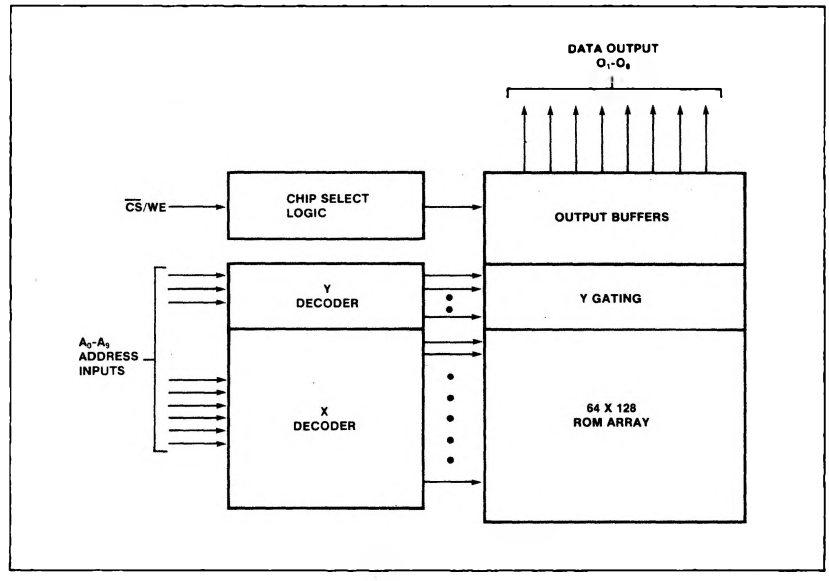
- **Organization:**
  **2708: 1024X8**
  **2704: 512X8**
- **Fast programming-100 sec. typ for all 8K bits**
- **Low power during programming**
- **Access time: 450ns**
- **Standard power supplies 12V, ±5V**
- **Static—no clocks required**
- **Inputs and outputs TTL compatible during both read and program modes**
- **Three-state output—OR-tie capability**

## PIN CONFIGURATION




*2708 = $A_9$
2704 = $V_{SS}$

## BLOCK DIAGRAM




## ABSOLUTE MAXIMUM RATINGS[1]

| | PARAMETER | RATING | UNIT |
|---|---|---|---|
| | Temperature range | | °C |
| $T_A$ | Operating | 0 to 70 | |
| $T_{STG}$ | Storage | -65 to 125 | |
| $P_D$ | Power dissipation | 1.5 | W |
| | All input or output voltage with respect to $V_{BB}$ (except program) | 15 to -0.3 | V |
| | Program input to $V_{BB}$ | 35 to -0.3 | V |
| | Supply voltages $V_{CC}$ and $V_{SS}$ with respect to $V_{BB}$ | 15 to -0.3 | V |
| | $V_{DD}$ with respect to $V_{BB}$ | 20 to -0.3 | V |

## DC ELECTRICAL CHARACTERISTICS

$V_{CC}$ = 5V ± .25V, $V_{BB}$ = -5V ± .25V, $V_{DD}$ = 12V ± .6V, $V_{SS}$ = 0V,
$T_A$ = 0°C to 70°C, Output load = 100pF plus 1TTL input.

| PARAMETER | | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[2] | Max | |
| | Input voltage | | | | | V |
| $V_{IL}$ | Low | | $V_{SS}$ | | 0.65 | |
| $V_{IH}$ | High | | 3.0 | | $V_{CC}$ + 1 | |
| | Output voltage | | | | | V |
| $V_{OL}$ | Low | $I_{OL}$ = 1.6mA | | | 0.45 | |
| $V_{OH1}$ | High | $I_{OH}$ = -100μA | 3.7 | | | |
| $V_{OH2}$ | High | $I_{OH}$ = -1mA | 2.4 | | | |
| $I_{LI}$ | Input load current | $V_{IH}$ = 5.25V | | | | μA |
| | Address and chip select | | | | 10 | |
| $I_{LO}$ | Output leakage current | $V_{OUT}$ = 5.25V, CS/WE = 5V | | | 10 | μA |
| | Supply current | Worst case supply currents, All inputs high | | | | mA |
| $I_{DD}$ | $V_{DD}$ | | | 50 | 65 | |
| $I_{CC}$ | $V_{CC}$ | | | 6 | 10 | |
| $I_{BB}$ | $V_{BB}$ | $\overline{CS}$/WE = 5V; $T_A$ = 0°C | | 30 | 45 | |
| $P_D$ | Power dissipation | $T_A$ = 70°C | | | 800 | mW |
| | Capacitance[3] | $T_A$ = 25°C, f = 1MHz | | | | pF |
| $C_{IN}$ | Input | $V_{IN}$ = 0V | | 4 | 6 | |
| $C_{OUT}$ | Output | $V_{OUT}$ = 0V | | 8 | 12 | |

## AC ELECTRICAL CHARACTERISTICS

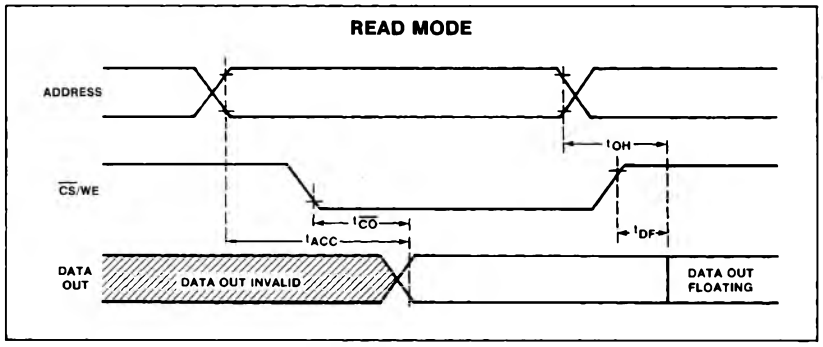
Output load = 1 TTL gate and CL = 100pF,
Input rise and fall times = 20ns,
Timing measurement reference levels = 0.8V and 2.8V for inputs,
0.8V and 2.4V for outputs. Input pulse levels = 0.65V to 3.0V

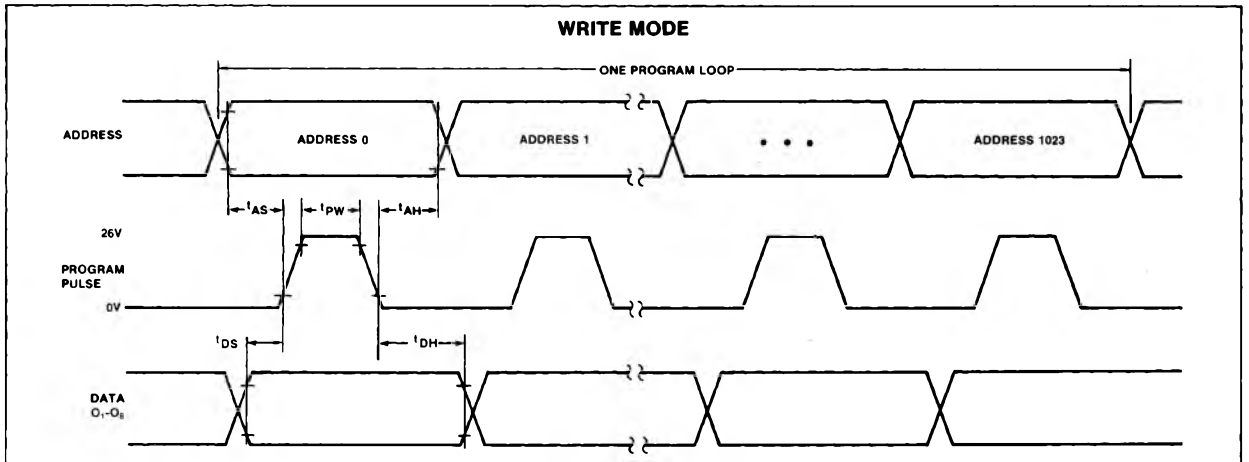
| PARAMETER | | TO | FROM | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| | Delay time | | | | | | ns |
| $t_{ACC}$ | | Output | Address | | 280 | 450 | |
| $t_{\overline{CO}}$ | | Output | Chip select | | | 120 | |
| $t_{DF}$ | Float time | Output | Chip deselect | 0 | | 120 | ns |
| $t_{OH}$ | Hold time | Output | Address | 0 | | | ns |

NOTES

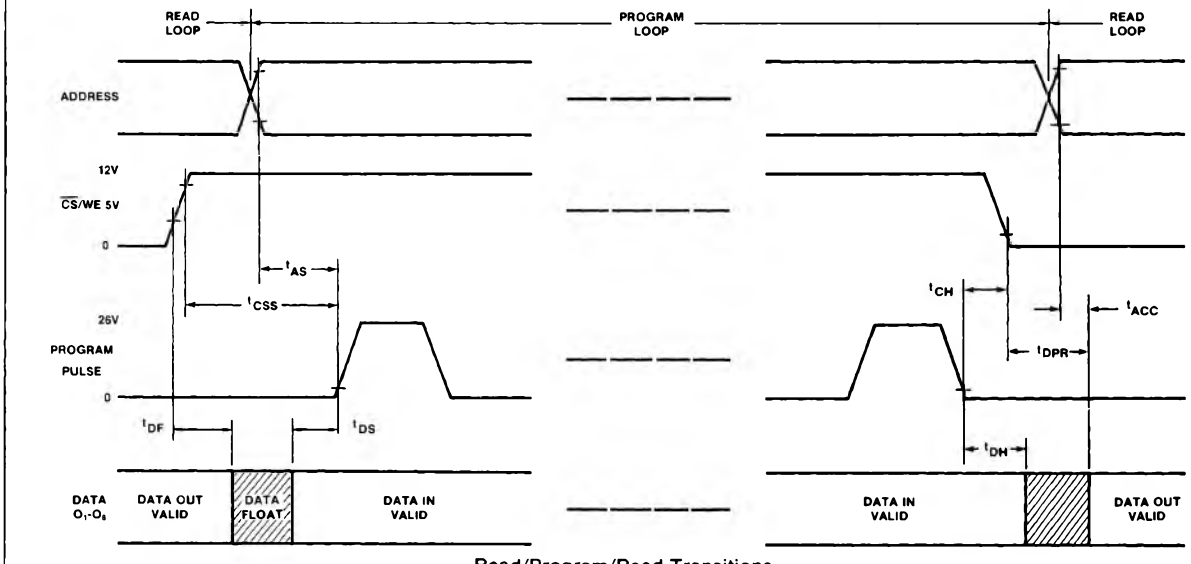
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Typical values are for $T_A$ = 25°C and typical supply voltages.
3. This parameter is periodically sampled and not 100% tested.
4. The program input (pin 18) may be tied to $V_{SS}$ during the read mode.
5. Signetics reserves the right to make changes in specification at any time and without notice. The information furnished by Signetics in this publication is believed to be accurate and reliable. However, no responsibility is assumed by Signetics for its use; nor any infringements of patents or other rights of third parties resulting from its use. No license is granted under any patents or patent rights of Signetics.

## TIMING DIAGRAMS




Program Mode: $\overline{CS}$/WE = +12V




Read/Program/Read Transitions

Logic levels and timing reference levels same as in the Read Mode unless noted otherwise.

## PROGRAMMING SPECIFICATIONS $T_A = 25°C$

| PARAMETER | | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| | Setup and hold time | | | | μs |
| $t_{AS}$ | Address setup | 10 | | | |
| $t_{AH}$ | Address hold | 1 | | | |
| $t_{CSS}$ | $\overline{CS}$/WE setup | 10 | | | |
| $t_{CH}$ | $\overline{CS}$/WE hold | .5 | | | |
| $t_{DS}$ | Data setup | 10 | | | |
| $t_{DH}$ | Data hold | 1 | | | |
| $t_{DF}$ | Chip deselect to output float delay | 0 | | 120 | ns |
| $t_{DPR}$ | Program to read delay | | | 10 | μs |
| $t_{PW}$ | Program pulse width | .1 | | 1.0 | ms |
| $t_{PR}$ | Program pulse rise time | .5 | | 2.0 | μs |
| $t_{PF}$ | Program pulse fall time | .5 | | 2.0 | μA |
| $I_P$ | Programming current | | 10 | 20 | mA |
| $V_P$ | Program pulse amplitude | 25 | | 27 | V |

## PROGRAMMING PROCEDURE

At shipment and after each erasure, all bits of the 2708/2704 are in the logic high state (output high). The device is put into the program mode by raising the $\overline{CS}$/WE input (pin 20) to +12V. While in the program mode, data to be stored is presented on lines $O_1$-$O_8$, forming an 8-bit word. Word addresses are selected in the same manner as in the Read mode. After each address and data word is set up, one program pulse ($V_P$) is applied to the program input (pin 18). Refer to the Program Mode timing diagram. A program loop is defined as one pass through all device addresses. The number of loops (N) required is dependent upon the program pulse width ($t_{PW}$) according to $N^* t_{PW} \geq 100ms$.

Program and read loops may be alternated as shown in the Read/Program/Read Transitions timing diagram.

## ERASING PROCEDURE

The 2708/2704 may be erased by exposure to high intensity short-wave ultraviolet light at a wavelength of $2537A_2°$. The recommended integrated dose (i.e., UV intensity x exposure time) is 10W-sec/cm$^2$. Examples of ultraviolet sources which can erase the 2708/2704 in 30 to 60 minutes are the Model UVS-54 and Model S-52 short-wave ultraviolet lamps manufactured by Ultra-Violet Products, Inc., 5114 Walnut Grove Avenue, San Gabriel, California. The lamps should be used without short-wave filters, and the 2708/2704 to be erased should be placed about 1 inch away from the lamp tubes. Both Cervue and UV glass lids are available.