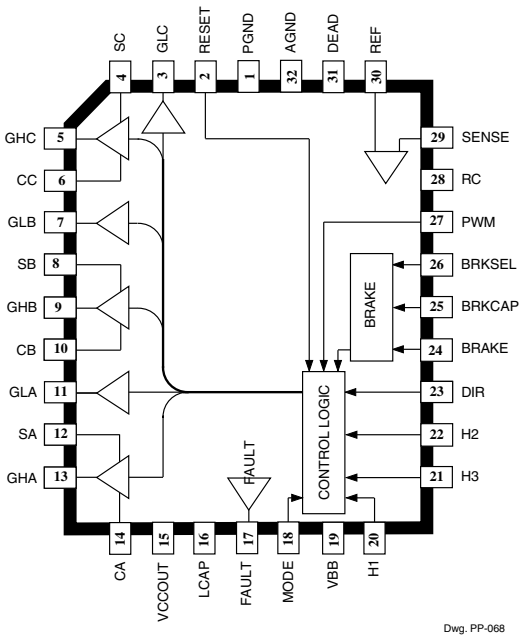
3933

Data Sheet
26301.100†

THREE-PHASE POWER MOSFET CONTROLLER



ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Supply Voltage, V_{BB} ..... **28 V**
(peak) ..... **30 V**
Terminal Voltage, V_{CCOUT} ..... **13.2 V**
(peak) ..... **15 V**
Logic Input Voltage Range,
V_{IN} ..... **-0.3 V to V_{LCAP} + 0.3 V**
Sense Voltage Range,
V_{SENSE} ..... **-5 V to V_{LCAP}**
Output Voltage Range,
V_{SA}, V_{SB}, V_{SC} ..... **-5 V to +30 V**
V_{GHA}, V_{GHB}, V_{GHC} . **-5 V to V_{BB} + 14 V**
V_{CA}, V_{CB}, V_{CC} ..... **V_{SX} + 14 V**
Operating Temperature Range,
T_A ..... **-20°C to +85°C**
Junction Temperature, T_J ..... **+150°C**
Storage Temperature Range,
T_S ..... **-55°C to +150°C**

The A3933SEQ is a three-phase MOSFET controller for use with bipolar brushless dc motors. It drives all n-channel external power FETs, allowing system cost savings and minimizing $r_{(DS)on}$ power loss. The high-side drive block is implemented with bootstrap capacitors at each output to provide the floating positive supply for the gate drive. The high-side circuitry also employs a unique "intelligent" FET monitoring circuit that ensures the gate voltages are at the proper levels before turn-on and during the ON cycle. This device is targeted for applications with motor supplies from 12 V to 28 V.

Internal fixed off-time PWM current-control circuitry can be used to regulate the maximum load current to a desired value. The peak load-current limit is set by the user's selection of an input reference voltage and external sensing resistor. The fixed off-time pulse duration is set by a user-selected external RC timing network.

A power-loss braking circuit brakes the motor on an under-voltage condition. The device is configured to either coast or dynamically brake the motor when this occurs.

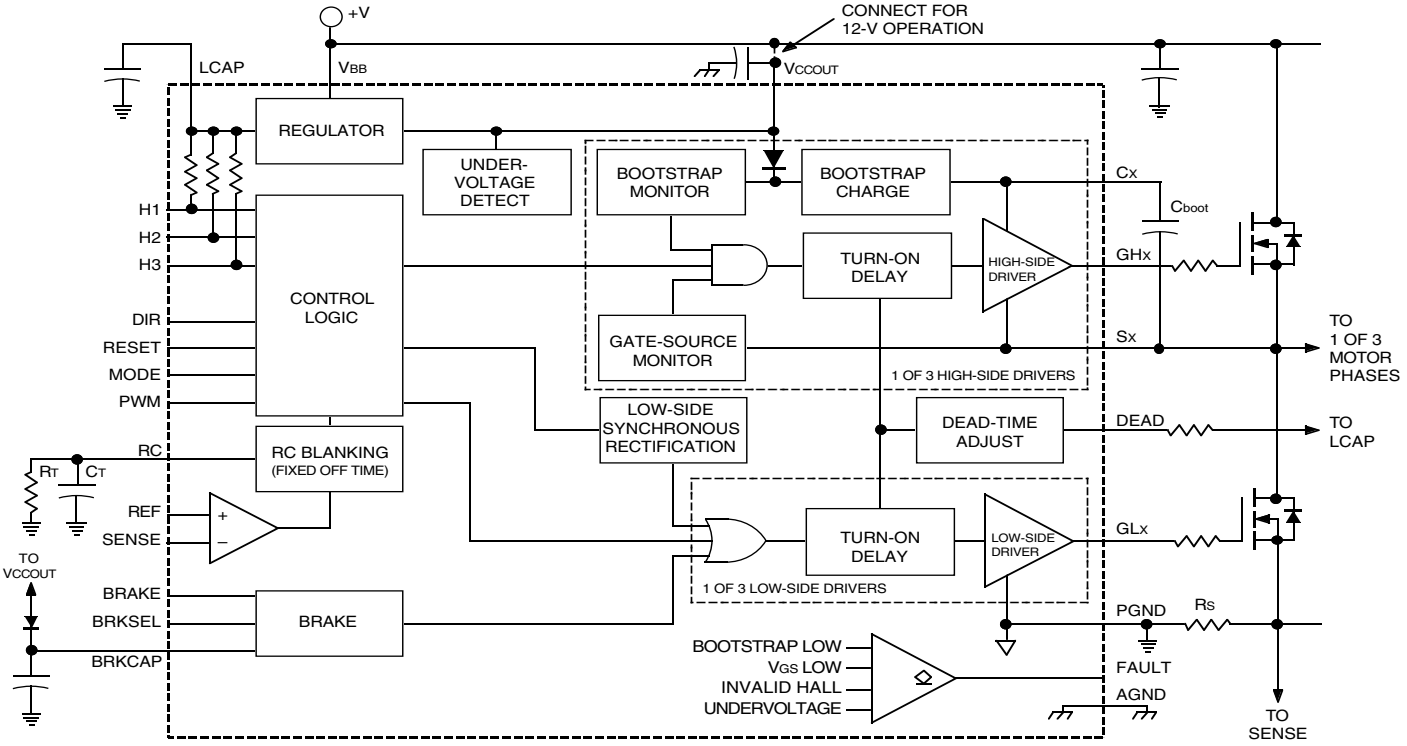
The A3933SEQ is supplied in a 32-lead rectangular (9 x 7) plastic chip carrier (quad pack) for minimum-area, surface-mount applications.

FEATURES AND BENEFITS

- Drives External N-Channel FETs
- Intelligent High-Side Gate Drive
- Selectable Coast or Dynamic Brake on Power Down
- Adjustable Dead Time for Cross-Conduction Protection
- Selectable Fast or Slow Current-Decay Modes
- Internal PWM Peak Current Control
- Reset/Coast Input
- 120° Hall Commutation with Internal Pullup
- Internal 5-V Regulator
- Low-Side Synchronous Rectification
- Direction Control
- PWM Speed-Control Input
- Fault-Diagnostic Output
- Under-Voltage Protection

3933
THREE-PHASE POWER MOSFET CONTROLLER

Functional Block Diagram



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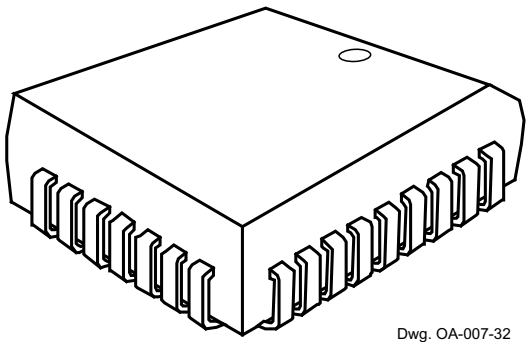

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RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{BB} ..... **15 V to 28 V**

or, if $V_{BB} = V_{CCOUT}$ ..... **12 V ±10%**

Logic Input Voltage Range, V_{IN} ..... **-0.3 V to +4.8 V**

Sense Voltage Range, V_{SENSE} ..... **-1 V to +1 V**

RC Resistance ..... **10 kΩ to 100 kΩ**

PWM Frequency, f_{PWM} ..... **20 kHz to 100 kHz**

Allegro MicroSystems, Inc.

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Worcester, Massachusetts 01615-0036 (508) 853-5000

ELECTRICAL SPECIFICATIONS at T_A = 25°C, V_{BB} = V_{CCOUT} = 12 V, C_{load} = 1000 pF, C_{boot} = 0.047 µF (unless noted otherwise).

Parameter	Symbol	Conditions	Limits			
			Min	Typ	Max	Units
Supply Current						
Quiescent Current	I_{BB}	RESET low, f_{PWM} = 40 kHz	–	16	19	mA
		RESET high	–	15	17	mA
Reference Voltage	V_{LCAP}		4.75	5.0	5.25	V
Ref. Volt. Load Regulation	$\Delta V_{LCAP(\Delta ILCAP)}$	I_{LCAP} = 0 to -2 mA	–	10	25	mV
Output Voltage	V_{CCOUT}	V_{BB} = 28 V	10.8	12	13.2	V
Output Voltage Regulation	$\Delta V_{CCOUT(\Delta ICCOUT)}$	V_{BB} = 28 V, I_{CCOUT} = 0 to -10 mA	–	–	25	mV
Digital Logic Levels						
Logic Input Voltage	V_{IH}		2.0	–	–	V
	V_{IL}		–	–	0.8	V
Logic Input Current	I_{IH}	V_{IH} = 2 V	–	<1.0	10	µA
	I_{IL}	V_{IL} = 0.8 V	-70	–	-130	µA
Gate Drive						
Low-Side Output Voltage	V_{GLxH}		9.5	10.5	11.5	V
	V_{GLxL}	I_{GLx} = 1 mA	–	–	0.30	V
High-Side Output Voltage	V_{GHxH}		9.0	10.5	11.5	V
	V_{GHxL}	I_{GHx} = 1 mA	–	–	0.25	V
Low-Side Output Switching Time	t_{rGLx}	1 V to 8 V	–	50	–	ns
	t_{fGLx}	8 V to 1 V	–	40	–	ns
High-Side Output Switching Time	t_{rGHx}	1 V to 8 V	–	100	–	ns
	t_{fGHx}	8 V to 1 V	–	100	–	ns
DEAD Time (Source OFF to Sink ON)	t_{DEAD}	I_{DEAD} = 10 µA	–	3000	–	ns
		I_{DEAD} = 215 µA	–	180	–	ns

Continued —

NOTES: 1. Typical Data is for design information only.
2. Negative current is defined as coming out of (sourcing) the specified device terminal.

ELECTRICAL SPECIFICATIONS at T_A = 25°C, V_{BB} = V_{CCOUT} = 12 V, C_{load} = 0.001 µF, C_{boot} = 0.047 µF (unless noted otherwise), continued.

Parameter	Symbol	Conditions	Limits			
			Min	Typ	Max	Units
Bootstrap Capacitor						
Bootstrap Charge Current	I_{Cx}		50	100	150	mA
Bootstrap Output Voltage	V_{Cx}	Reference Sx	9.5	10.5	11.5	V
Leakage Current	I_{Cx}	High side switched high, Sx = V_{BB}	–	15	20	µA
Current Limit						
Offset Voltage	V_{io}		–	0	±5.0	mV
Input bias current	I_{SENSE}		–	–	-1.0	µA
RC Charge Current	I_{RC}		850	945	1040	µA
RC Voltage Threshold	V_{RCL}		1.0	1.1	1.2	V
	V_{RCH}		2.7	3.0	3.2	V
PWM frequency Range	f_{PWM}	Operating	20	–	100	kHz
Protection Circuitry						
Undervoltage Threshold	UVLO	Increasing V_{BB}	9.7	10.2	10.7	V
		Decreasing V_{BB}	9.35	–	10.35	V
Boot-Strap Capacitor Volt.	V_{CxSx}	V_{BB} = 12 V	9.5	–	–	V
High-Side Gate-Source Volt.	V_{GHxSx}		–	6.3	–	V
Fault Output Voltage	V_{FAULT}	I_O = 1 mA	–	–	0.8	V
Brake Function						
Brake Cap. Supply Current	I_{BRKCAP}	V_{BB} = 8 V, BRKSEL ≥ 2 V	–	30	–	µA
Low-Side Gate Voltage	V_{GLxH}	V_{BB} = 0, BRKCAP = 8 V	–	6.6	–	V

NOTES: 1. Typical Data is for design information only.
2. Negative current is defined as coming out of (sourcing) the specified device terminal.

Terminal Descriptions

Terminal	Name
1	PGND
2	RESET
3	GLC
4	SC
5	GHC
6	CC
7	GLB
8	SB
9	GHB
10	CB
11	GLA
12	SA
13	GHA
14	CA
15	V_{CCOUT}
16	LCAP
17	FAULT
18	MODE
19	V_{BB}
20	H1
21	H3
22	H2
23	DIR
24	BRAKE
25	BRKCAP
26	BRKSEL
27	PWM
28	RC
29	SENSE
30	REF
31	DEAD
32	AGND

RESET — A logic input used to enable the device, internally pulled up to V_{LCAP} (+5 V). A logic HIGH will disable the device and force all gate drivers to 0 V, coasting the motor. A logic LOW allows the gate drive to follow commutation logic. This input overrides BRAKE.

GLA/GLB/GLC — Low-side, gate-drive outputs for external NMOS drivers. External series-gate resistors (as close as possible to the NMOS gate) can be used to control the slew rate seen at the power-driver gate, thereby controlling the di/dt and dv/dt of the SA/SB/SC outputs. Each output is designed and specified to drive a 1000 pF load with a rise time of 50 ns.

SA/SB/SC — Directly connected to the motor, these terminals sense the voltages switched across the load. These terminals are also connected to the negative side of the bootstrap capacitors and are the negative supply connections for the floating high-side drive.

GHA/GHB/GHC — High-side, gate-drive outputs for external NMOS drivers. External series-gate resistors (as close as possible to the NMOS gate) can be used to control the slew rate seen at the power-driver gate, thereby controlling the di/dt and dv/dt of the SA/SB/SC outputs. Each output is designed and specified to drive a 1000 pF load with a rise time of 100 ns.

CA/CB/CC — High-side connections for the bootstrap capacitors, positive supply for high-side gate drive. The bootstrap capacitor is charged to approximately V_{CCOUT} when the associated output SA/SB/SC terminal is low. When the output swings high, the voltage on this terminal rises with the output to provide the boosted gate voltage needed for n-channel power FETs.

continued next page

Terminal Descriptions (cont'd)

FAULT — Open-drain output to indicate fault condition; will go active high for any of the following:

1 – invalid HALL input code,

2 – high-side, gate-source voltage less than 7 V,

3 – bootstrap capacitor not sufficiently charged, or

4 – under-voltage condition detected at V_{CCOUT}.

The fault state for gate-source and bootstrap monitors are cleared at each commutation. If the motor has stalled, then the fault can only be cleared by toggling the RESET terminal or power-up sequence.

MODE — A logic input to set current-decay method, internally pulled up to V_{LCAP} (+5 V). When in slow-decay mode (logic HIGH), only the high-side FET is switched open during a PWM OFF cycle. The fast-decay mode (logic LOW) switches both the source and sink FETs.

H1/H2/H3 — Hall-sensor inputs; internally pulled up to V_{LCAP} (+5 V). Configured for 120° electrical spacing.

DIR — A logic input to reverse rotation, see commutation logic table. Internally pulled up to V_{LCAP} (+5 V).

BRAKE — A logic input to short out the motor windings for a braking function. A logic HIGH will turn ON the low-side FETs, turn OFF the high-side FETs. Internally pulled up to V_{LCAP} (+5 V). The braking torque applied will depend on the speed.

BRKCAP — Connection for reservoir capacitor. This terminal is used to provide a positive power supply for the sink-drive outputs for a power-down condition. This will allow predictable braking, if desired. A blocking diode to V_{CCOUT} is required. A 4.7 µF capacitor will provide 6.5 V gate drive for 300 ms. If a power-down braking option is not needed (BRKSEL = LOW) then this terminal should be tied to V_{CCOUT}.

BRKSEL — A logic input to enable/disable braking on power-down condition. Internally pulled up to V_{LCAP} (+5 V). If held low, the motor will coast on a power-down condition.

PWM — Speed control input, internally pulled up to V_{LCAP} (+5 V). A logic LOW turns OFF all drivers, a logic HIGH will turn ON selected drivers as determined by H1/H2/H3 input logic. Holding the terminal high allows speed/torque control solely by the current-limit circuit via REF analog voltage command.

RC — An analog input used to set the fixed off time with an external resistor (R_T) and capacitor (C_T). The t_{blank} time is controlled by the value of the external capacitor (see Applications Information). As a rule, the fixed off time should not be less than 10 µs. The resistor should be in the range of 10 kΩ to 100 kΩ.

SENSE — An analog input to the current-limit comparator. A voltage representing load current appears on this terminal during ON time, when it reaches REF voltage, the comparator trips and load current decays for the fixed off-time interval. Voltage transients seen at this terminal when the drivers turn ON are ignored for time t_{blank}.

REF — An analog input to the current-limit comparator. Voltage applied here sets the peak load current.

$$I_{peak} = V_{REF}/R_S.$$

V_{CCOUT} — A regulated 12 V output; supply for low-side gate drive and bootstrap capacitor charge circuits. It is good practice to connect a decoupling capacitor from this terminal to AGND, as close to the device terminals as possible. The terminal should be shorted to V_{BB} for 12 V applications.

V_{BB} — The A3933 supply voltage. It is good practice to connect a decoupling capacitor from this terminal to AGND, as close to the device terminals as possible. This terminal should be shorted to V_{CCOUT} for 12 V applications.

LCAP — Connection for decoupling capacitor for the internal 5 V reference. This terminal can source no more than 2 mA.

DEAD — An analog input. A resistor between DEAD and LCAP is selected to adjust turn-off to turn-on time. This delay is needed to prevent shoot-through in the external power FETs. The allowable resistor range is 20 kΩ to 430 kΩ, which converts to deadtime of 210 ns to 2.1 µs, using the following equation:

$$t_{DEAD} = (6.75 \times 10^{-12} \times R_{DEAD}) + (75 \times 10^{-9}).$$

AGND — The low-level (analog) reference point for the A3933.

PGND — The reference point for all low-side gate drivers.

Commutation Truth Table

Logic Inputs				Driver Outputs								
H1	H2	H3	DIR	GLA	GLB	GLC	GHA	GHB	GHC	SA	SB	SC
H	L	H	H	L	L	H	H	L	L	H	Z	L
H	L	L	H	L	L	H	L	H	L	Z	H	L
H	H	L	H	H	L	L	L	H	L	L	H	Z
L	H	L	H	H	L	L	L	L	H	L	Z	H
L	H	H	H	L	H	L	L	L	H	Z	L	H
L	L	H	H	L	H	L	H	L	L	H	L	Z
H	L	H	L	H	L	L	L	L	H	L	Z	H
H	L	L	L	L	H	L	L	L	H	Z	L	H
H	H	L	L	L	H	L	H	L	L	H	L	Z
L	H	L	L	L	L	H	H	L	L	H	Z	L
L	H	H	L	L	L	H	L	H	L	Z	H	L
L	L	H	L	H	L	L	L	H	L	L	H	Z

Input Logic

MODE	PWM	RESET	Mode	Operation
L	L	L	Fast decay	PWM chop mode, current decay
L	H	L	Fast decay	Peak current limit, selected drivers ON
H	L	L	Slow decay	PWM chop mode. current decay
H	H	L	Slow decay	Peak current limit, selected drivers ON
X	X	H	Coast	All gate drive outputs OFF, clear fault logic

Brake Control

BRAKE	BRKSEL	Normal Operation	Under Voltage or Power Loss Condition
L	L	Normal run mode	Coast, all gate drive outputs OFF
L	H	Normal run mode	Dynamic brake, all sink gate drives ON
H	L	Dynamic brake, all sink gate drives ON	Coast, all gate drive outputs OFF
H	H	Dynamic brake, all sink gate drives ON	Dynamic brake, all sink gate drives ON

L = Low Level, H = High Level, X = Don't Care, Z = High Impedance

Applications Information

Bootstrap Capacitor Selection. The high-side bootstrap circuit operates on a charge-transfer principle. The gate charge (Q_g) specification of the external power MOSFET must be taken into consideration. The bootstrap capacitor must be large enough to turn on the MOSFET without losing significant gate voltage. If the bootstrap capacitor is too large, it would take too long to charge up during the off portion of the PWM cycle. The capacitor value must be selected with both of these constraints in mind.

1) Minimum bootstrap capacitor value to transfer charge. The charge on the bootstrap capacitor should be 20x greater than the gate charge (Q_g) of the power MOSFET.
Example: For Q_g = 0.025 µC, select

$$C_{boot} = 20 \times Q_g/10.5\ V = 0.047\ \mu F.$$

Check for maximum V_g drop at turn on: $dq = C_{boot} \times dV_g$, where $Q_g = dq$.

$$dV_g = dq/C_{boot} = 0.025\ \mu C/0.047\ \mu F = 532\ mV.$$

2) Calculate minimum PWM "OFF" cycle with C_{boot} = 0.047 µF.

$$dt = r_o \times C_{boot} \times \ln(0.036/[Q_g/C_{boot} + 0.036])$$

where r_o = 20 ohms, the equivalent internal series resistance of the bootstrap capacitor monitor circuit.

The sink-side MOSFET will be held OFF for this minimum time such that the bootstrap capacitor can be recharged independently of the PWM input frequency.

The above equation is valid for PWM cycles after the bootstrap capacitor has been charged once. For the first cycle after a motor phase commutates from Hi-Z to GHx ON, or during the first charging cycle at power-up, the circuit will ignore PWM signals until it has been charged.

The time required to charge up at power up and at commutation change is approximately:

$$t = C_{boot} \times 7\ V/0.1\ A$$

Protection Circuitry. The A3933 will protect the external MOSFETs by shutting down the gate drive if any of the following conditions are detected:

1) **Gate Source Monitor (high side only).** The voltage on the GHx terminals must stay 7 V higher than the source. If this voltage droops below the threshold, the high side turns OFF, and the low-side gate will turn ON in an attempt to recharge the bootstrap capacitor. When the bootstrap capacitor has been properly charged, the high side is turned back ON. The circuit will allow three faults of this type within one commutation cycle before signaling a fault and coast the motor (all gate outputs go low).

2) **Bootstrap Monitor.** The bootstrap capacitor is charged whenever a sink-side MOSFET is ON, Sx output goes low, and the load current recirculates. This happens constantly during normal operation. A 60 µs timer is started at the beginning of this cycle and the capacitor is charged with typically 100 mA. The bootstrap capacitor voltage is clamped at approximately 87% of V_{CCOUT}. If the capacitor is not charged to the clamp voltage in 60 µs, a fault is signaled and the motor will coast.

3) **Undervoltage.** The internal V_{CCOUT} regulator supplies the low-side gate driver and the bootstrap charge current. It is critical to ensure that the voltages are at a proper level before enabling any of the outputs. The undervoltage circuit is active during power up and will force a motor coast condition until V_{CCOUT} is greater than approximately 10 V.

4) **Hall Invalid.** Illegal codes for the HALL inputs (000 or 111) will force a fault and coast the motor.

Faults are cleared at the beginning of each commutation. If a stalled motor results from a fault, the fault can only be cleared by toggling the RESET terminal or by a power-up sequence.

Current Control. Internal fixed off-time PWM circuitry is implemented to limit load current to a desired value. The external sense resistor combined with the applied analog voltage to REF terminal will set the peak current level approximately

$$I_{TRIP} \approx V_{REF}/R_S.$$

After the peak level is reached, the sense comparator trips and the load current will decay for a fixed off time.

An external resistor (R_T) and capacitor (C_T) are used to set the fixed off-time period ($t_{off} = R_T \times C_T$). The t_{off} should be in the range of 10 µs to 50 µs. Longer values for t_{off} can result in audible noise problems.

Torque control can be implemented by varying the REF input voltage as long as the PWM input stays high. If direct control of the torque/current is desired by PWM input, a voltage can be applied to the REF input to set an absolute maximum current limit.

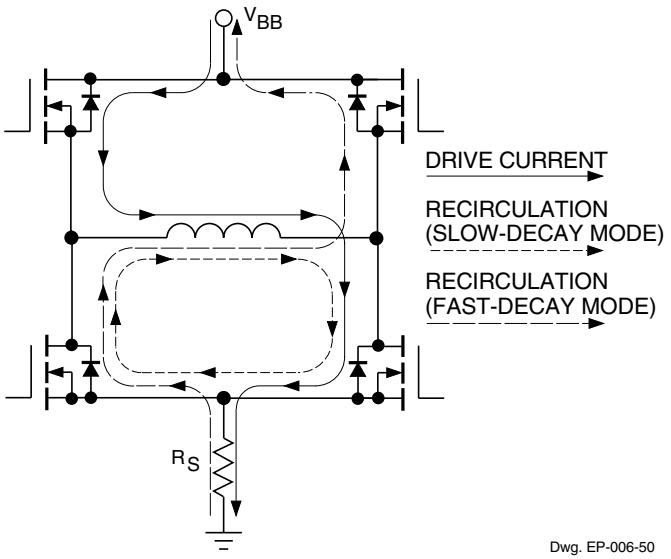
Applications Information (cont'd)

PWM Blank. The capacitor (C_T) also serves as the means to set the blank time duration. After the off time expires, the selected gates are turned back ON. At this time, large current transients can occur during the reverse recovery time (t_{rr}) of the intrinsic body diodes of the external MOSFETs. To prevent the current-sense comparator from thinking the current spikes are a real overcurrent event, the comparator is blanked:

$$t_{blank} = 1.9 \times C_T/(1\ mA\text{-}2/R_T)$$

The user must ensure that C_T is large enough to cover the current-spike duration.

Load Current Recirculation. If MODE has been set for slow decay, the high-side (source) driver will turn OFF forcing the current to recirculate through the pair of sink MOSFETs. If MODE has been selected for fast decay, both the selected high- and low-side gates are turned OFF, which will force the current to recirculate through one sink MOSFET and the high-side clamp diode. Synchronous rectification (only on the low side) allows current to flow through the MOSFET, rather than the clamp diode, during the decay time. This will minimize power loss during the off period. It is important to take into account that, when switching, the intrinsic diodes will conduct during the adjustable deadtime.



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Braking. The A3933 will dynamically brake by forcing all sink-side MOSFETs ON. This will effectively short out the BEMF. During braking, the load current can be approximated by:

$$I_{BRAKE} = V_{BEMF}/R_L$$

Power Loss Brake. The BRKCAP and BRKSEL terminals provide a power-down braking option. By applying a logic level to input BRKSEL, the system can control if the motor is dynamically braked or is allowed to coast during an undervoltage event. The reservoir capacitor on the BRKCAP terminal provides the power to hold the sink-side gates ON after supply voltage is lost. A logic high on BRKSEL will brake the motor, a logic low and it will coast.

Layout. Careful consideration must be given to PCB layout when designing high-frequency, fast-switching, high-current circuits.

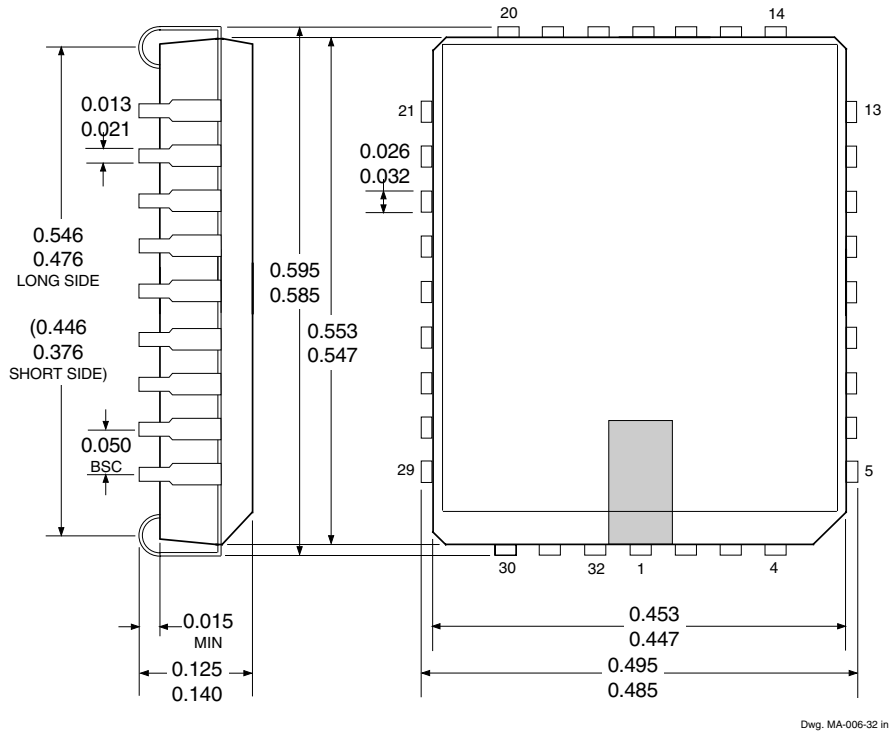
1) The analog ground (AGND), the power ground (PGND), and the high-current return of the external MOSFETs (the negative side of the sense resistor) should return separately to the negative side of the motor supply filtering capacitor. This will minimize the effect of switching noise on the device logic and analog reference.

2) Minimize stray inductances by using short, wide copper runs at the drain and source terminals of all power MOSFETs. This includes motor lead connections, the input power buss, and the common source of the low-side power MOSFETs. This will minimize voltages induced by fast switching of large load currents.

3) Kelvin connect the SENSE terminal PC trace to the positive side of the sense resistor.

Dimensions in Inches

(controlling dimensions)

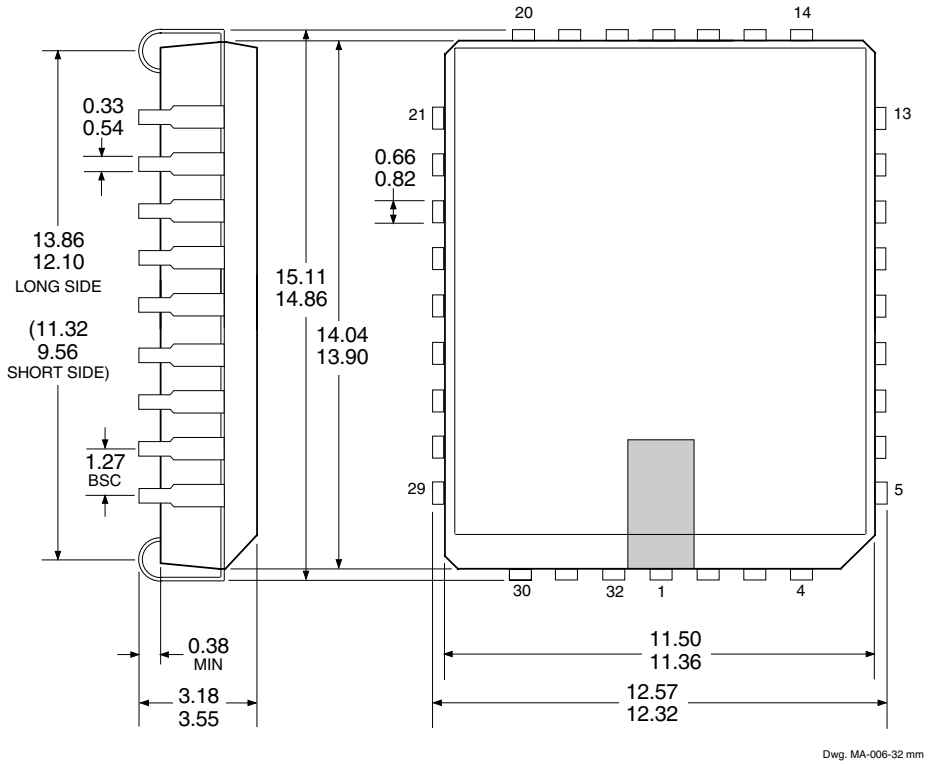


NOTES: 1. Lead spacing tolerance is non-cumulative.

2. Exact body and lead configuration at vendor's option within limits shown

Dimensions in Millimeters

(for reference only)



NOTES: 1. Lead spacing tolerance is non-cumulative.

2. Exact body and lead configuration at vendor's option within limits shown

3933
THREE-PHASE POWER MOSFET CONTROLLER

MOTOR DRIVERS

Function	Output Ratings*		Part Number†
INTEGRATED CIRCUITS FOR BRUSHLESS DC MOTORS			
3-Phase Power MOSFET Controller	—	28 V	3933
3-Phase Power MOSFET Controller	—	50 V	3932
3-Phase Power MOSFET Controller	—	50 V	7600
2-Phase Hall-Effect Sensor/Driver	400 mA	26 V	3626
Bidirectional 3-Phase Back-EMF Controller/Driver	±600 mA	14 V	8906
2-Phase Hall-Effect Sensor/Driver	900 mA	14 V	3625
3-Phase Back-EMF Controller/Driver	±900 mA	14 V	8902–A
3-Phase Controller/Drivers	±2.0 A	45 V	2936 & 2936-120
INTEGRATED BRIDGE DRIVERS FOR DC AND BIPOLAR STEPPER MOTORS			
Dual Full Bridge with Protection & Diagnostics	±500 mA	30 V	3976
PWM Current-Controlled Dual Full Bridge	±650 mA	30 V	3966
PWM Current-Controlled Dual Full Bridge	±650 mA	30 V	3968
PWM Current-Controlled Dual Full Bridge	±750 mA	45 V	2916
PWM Current-Controlled Dual Full Bridge	±750 mA	45 V	2919
PWM Current-Controlled Dual Full Bridge	±750 mA	45 V	6219
PWM Current-Controlled Dual Full Bridge	±800 mA	33 V	3964
PWM Current-Controlled Full Bridge	±1.3 A	50 V	3953
PWM Current-Controlled Dual Full Bridge	±1.5 A	45 V	2917
PWM Current-Controlled Dual Full Bridge	±1.5 A	45 V	2918
PWM Current-Controlled Microstepping Full Bridge	±1.5 A	50 V	3955
PWM Current-Controlled Microstepping Full Bridge	±1.5 A	50 V	3957
PWM Current-Controlled Dual DMOS Full Bridge	±1.5 A	50 V	3972
Dual Full-Bridge Driver	±2.0 A	50 V	2998
PWM Current-Controlled Full Bridge	±2.0 A	50 V	3952
DMOS Full Bridge PWM Driver	±2.0 A	50 V	3958
Dual DMOS Full Bridge	±2.5 A	50 V	3971
UNIPOLAR STEPPER MOTOR & OTHER DRIVERS			
Voice-Coil Motor Driver	±500 mA	6 V	8932–A
Voice-Coil Motor Driver	±800 mA	16 V	8958
Unipolar Stepper-Motor Quad Drivers	1 A	46 V	7024 & 7029
Unipolar Microstepper-Motor Quad Driver	1.2 A	46 V	7042
Unipolar Stepper-Motor Translator/Driver	1.25 A	50 V	5804
Unipolar Stepper-Motor Quad Driver	1.8 A	50 V	2540
Unipolar Stepper-Motor Quad Driver	1.8 A	50 V	2544
Unipolar Stepper-Motor Quad Driver	3 A	46 V	7026
Unipolar Microstepper-Motor Quad Driver	3 A	46 V	7044

* Current is maximum specified test condition, voltage is maximum rating. See specification for sustaining voltage limits or over-current protection voltage limits. Negative current is defined as coming out of (sourcing) the output.

† Complete part number includes additional characters to indicate operating temperature range and package style.

Also, see 3175, 3177, 3235, and 3275 Hall-effect sensors for use with brushless dc motors.

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