Intel® 440MX Chipset

Electrical and Thermal Specification

Datasheet Addendum

Product Features

- Processor Host Bus Support
  - —Optimized for these 100 MHz or 66 MHz processors:
    - – Mobile Intel® Pentium® III Processor
    - – Intel®Pentium III Processor – Low Power
    - – Intel® Celeron™ Processor
    - – Intel®Celeron™ Processor – Low Power
  - —GTL+ Bus Driver Technology
- Integrated DRAM Support
  - —8 Mbytes to 256 Mbytes using 16-Mbit, 64-Mbit, and 128-Mbit Technology
  - —Standard and Registered SDRAM (Synchronous) DRAM Support (x-1-1-1 access at 100 MHz or 66 MHz)
  - —Enhanced Open Page Arbitration SDRAM Paging Scheme
- PCI Bus Interface
  - —PCI Rev. 2.3, 3.3-V, 33-MHz Interface Compliant
- Integrated IDE Controller
  - —One Channel Support for “Ultra DMA/33” Synchronous DMA Mode
- System Peripheral Support
  - —Enhanced DMA Controller Support for Dual Cascaded 82C37 Controllers
  - —Interrupt Controller based on two 82C59 for up to 15 Interrupts
  - —System Timer based on 82C54
  - —Real Time Clock with 256-bytes battery-backed RAM
- X-bus Support for SIO, KBCX, and Flash
- USB
  - —AC’97 Link Controller
- AC’97 Audio Modem CODEC Interface Support
  - —USB 1.1 Port for Serial Transfers at 12 or 1.5 Mbits/s
  - —Supports UHCI Design Guide
- SMBus Support
- Power Management Logic
  - —Support for Power-On-Suspend, Suspend-To-SDRAM, and Suspend-To-Disk
  - —Support for Thermal Alarm
  - —Full Support for *ACPI Specification Revision 1.0*
- 31 GPIO Pins
- Thermal Design Power
  - —2.1 W for 100 MHz
  - —1.65 W for 66 MHz
- 492 µBGA Package

The Intel® 440MX chipset integrates the traditional north bridge and south bridge into one device, reducing power and board space for Mobile and low power Pentium III and Celeron processor designs.

Order Number: 273502-001
March 2001

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Revision History

Date	Revision	Description
March 2001	001	First release of this document.

1.0 Introduction

This document contains the electrical and thermal specifications for the Intel®440MX chipset.

The 440MX chipset is a single-component embedded chipset that is optimized for the Mobile Intel® Celeron™ Processor, Celeron™ Processor – Low Power, Mobile Pentium® III Processor, and Pentium® III Processor – Low Power for mobile and applied computing platforms. The 440MX chipset reduces the number of chipset components without requiring any major programming model changes. It accomplishes this by integrating the 82443BX Host/Bridge Controller (north bridge without AGP) and the 82371EB PIIX4E (south bridge) and adding a two-channel, digital AC'97 link feature. This single-component chipset is specifically designed to reduce system cost, space, and power. The 440MX chipset is packaged in a 492 µBGA package.

1.1 References

Intel® 440MX-100 PCIset datasheet (order number 245292)

Universal Host Controller Interface (UHCI) Design Guide, Rev 1.1 (order number 297650)

ATA Synchronous DMA Transfer Protocol (Proposal), Rev 0.40, Quantum Corp.

System Management Bus Specification, Rev 1.0

PCI 3.3 Signaling Environment DC and AC Specifications

AC'97 Rev 2.0 Specification

PCI Local Bus Specification, Revision 2.2.

2.0 Electrical Characteristics

2.1 DC Characteristics

Table 1. 440MX DC Characteristics (Sheet 1 of 3)

Functional Operating Range REFV_{CC} = 5 V ± 5%, V_{CC}=3.3 V ± 5%, T_{CASE} = 0° C to +95° C)

Symbol	Parameter	Min	Max	Unit	Notes
$V_{CC(RTC)}$	Battery Voltage	2.0	3.6	V	
$V_{CC(SUS)}$	Standby Voltage	3.0	3.6	V	
V_{IL1}	Input Low Voltage	-0.5	0.3 V_{CC}	V	1
V_{IH1}	Input High Voltage	0.5 V_{CC}	V_{CC} + 0.5	V	1
V_{IL2}	Input Low Voltage	-0.3	0.6	V	1
V_{IH2}	Input High Voltage	1.4	V_{CC} + 0.3	V	1
V_{IL3}	Input Low Voltage	-0.5	0.8	V	1
V_{IH3}	Input High Voltage	2.0	V_{CC}5 + 0.5	V	1
V_{IL4}	Input Low Voltage	- 0.3	0.8	V	1, 3
V_{IH4}	Input High Voltage	2.0	V_{CC} + 0.3	V	1, 3
V_{IL5}	GTL+ Input Low Voltage	-0.3	GTL_REF - 0.2	V	1, 4
V_{IH5}	GTL+ Input High Voltage	GTL_REF + 0.2	1.835	V	1, 4
V_{IL6}	PCI (3.3V) Open Drain Input Low Voltage	-0.3	0.8	V	1, 3
V_{IH6}	PCI (3.3V) Open Drain Input High Voltage	2.0	V_{CC} + 0.3	V	1, 3
V_{IL7}	AC'97 Input Low Voltage	-0.5	0.35 V_{CC}	V	1, 3
V_{IH7}	AC'97 Input High Voltage	0.65 V_{CC}	V_{CC} +0.5	V	1, 3
V_{OL1}	Output Low Voltage		0.4	V	1
V_{OH1}	Output High Voltage	V_{CC} - 0.5		V	1
V_{OL2}	Output Low Voltage		0.3	V	1, 2
V_{OH2}	Output High Voltage	2.8	3.6	V	1, 2
V_{OL3}	Output Low Voltage		0.45	V	1
V_{OH3}	Output High Voltage	V_{CC} - 0.5		V	1
V_{OL4}	Output Low Voltage		0.4	V	1

NOTES:
1. Refer to Table 2 for the signals associated with this specification.
2. V_{OL2} assumes R_L of 1.5 kΩ to 3.6V and V_{OH2} assumes R_L of 15 kΩ to GND.
3. During transitions, the inputs may overshoot beyond max V_{CC} or undershoot below V_{SS} by 0.8V for 7.0 ns on the 440MX inputs, with a maximum instantaneous overshoot/undershoot of ± 1.6V.
4. During transitions, the inputs may overshoot/undershoot beyond V_{TTmax} or below V_{SS} by ± 0.3V (violating the overshoot/undershoot guideline is acceptable, although satisfying the ringback specification will be very difficult as a result). Maximum rising edge ringback is 1.12V. Maximum falling edge ringback is 0.88V.
5. Parameter correlated into a 120 Ω resistor.
6. For 0.25µ Mobile Pentium II and Celeron processor designs.
7. For 0.18µ Mobile Pentium III and Celeron processor designs.

Table 1. 440MX DC Characteristics (Sheet 2 of 3)

Functional Operating Range $REFV_{CC}$ = 5 V ± 5%, V_{CC}=3.3 V ± 5%, T_{CASE} = 0° C to +95° C)

Symbol	Parameter	Min	Max	Unit	Notes
V_{OH4}	Output High Voltage	2.4		V	1
V_{OL5}	GTL+ Output Low Voltage		0.6	V	1, 5
V_{OL6}	PCI Open Drain Output Low Voltage		0.4	V	1
V_{OL7}	AC'97 Output Low Voltage		0.1 V_{CC}	V	1
V_{OH7}	AC'97 Output High Voltage	0.9 V_{CC}		V	1
GTL_REF	GTL+ Reference Voltage	5/9 V_{TT} - 2%	5/9 V_{TT} + 2%	V	1, 6
GTL_REF	GTL+ Reference Voltage	2/3 V_{TT} - 2%	2/3 V_{TT} + 2%	V	1, 7
V_{TT}	GTL+ Termination Voltage	1.465	1.835	V	1
$REFV_{CC}$	5V Reference	4.75	5.25	V	1
V_{DI}	Differential Input Sensitivity	0.2		V	|(USBPRTx+, USBPRTx-)|
V_{CM}	Differential Common Mode Range	0.8	2.5	V	Includes V_{DI}
V_{SE}	Single Ended Rcvr Threshold	0.8	2.0	V	
I_{OL1}	Output Low Current		4	mA	1, @ V_{OL1}
I_{OH1}	Output High Current	-1		mA	1, @ V_{OH1}
I_{OL2}	Output Low Current		10	mA	1, @ V_{OL4}
I_{OH2}	Output High Current	-3		mA	1, @ V_{OH4}
I_{OL3}	CMOS Output Low Current		3	mA	1, @ V_{OL1}
I_{OH3}	CMOS Output High Current	-2		mA	1, @ V_{OH1}
I_{OL4}	Output Low Current		6	mA	1, @ V_{OL1}
I_{OH4}	Output High Current	-2		mA	1, @ V_{OH1}
I_{OL5}	Output Low Current		2	mA	1, @ V_{OL2}
I_{OH5}	Output High Current	-0.25		mA	1, @ V_{OH2}
I_{OL6}	Output Low Current		7	mA	1, @ V_{OL1}
I_{OH6}	Output High Current	-2		mA	1, @ V_{OH1}
I_{OL7}	GTL+ Output Low Current		9	mA	1, @ VOL5
I_{OL8}	AC'97 Output Low Current		0.1 V_{CC}	mA	1, @ V_{OL7}
I_{OH8}	AC'97 Output High Current	0.9 V_{CC}		mA	1, @ V_{OH7}
I_{IL1}	Input Leakage Low Current		- 10	µA	
I_{IH1}	Input Leakage High Current		+ 10	µA	

NOTES:
1. Refer to Table 2 for the signals associated with this specification.
2. V_{OL2} assumes R_L of 1.5 kΩ to 3.6V and V_{OH2} assumes R_L of 15 kΩ to GND.
3. During transitions, the inputs may overshoot beyond max V_{CC} or undershoot below V_{SS} by 0.8V for 7.0 ns on the 440MX inputs, with a maximum instantaneous overshoot/undershoot of ± 1.6V.
4. During transitions, the inputs may overshoot/undershoot beyond V_{TTmax} or below V_{SS} by ± 0.3V (violating the overshoot/undershoot guideline is acceptable, although satisfying the ringback specification will be very difficult as a result). Maximum rising edge ringback is 1.12V. Maximum falling edge ringback is 0.88V.
5. Parameter correlated into a 120 Ω resistor.
6. For 0.25µ Mobile Pentium II and Celeron processor designs.
7. For 0.18µ Mobile Pentium III and Celeron processor designs.

Table 1. 440MX DC Characteristics (Sheet 3 of 3)

Functional Operating Range REFV_{CC} = 5 V ± 5%, V_{CC}=3.3 V ± 5%, T_{CASE} = 0° C to +95° C)

Symbol	Parameter	Min	Max	Unit	Notes
C_{IN0}	Input Capacitance		12	pF	F_C= 1 MHz
C_{IN1}	Input Capacitance		4	pF	F_C= 1 MHz
C_{IN2}	HCLKIN Input Capacitance	6.4	9.8	pF	F_C= 1 MHz
C_{IN3}	DCLK Input Capacitance	7.4	11.1	pF	F_C= 1 MHz
C_{IN4}	MD[63:0] Input Capacitance	6.5	10.6	pF	F_C= 1 MHz
C_{IN5}	PCICLK Input Capacitance	7.7	11.6	pF	F_C= 1 MHz
C_{OUT1}	Output Capacitance	6.6	11.3	pF	F_C= 1 MHz
C_{OUT2}	DCLKO Output Capacitance	6.6	10.1	pF	F_C= 1 MHz
$C_{I/O}$	I/O Capacitance		12	PF	F_C= 1 MHz
$C_{I/O1}$	I/O Capacitance	6.7	10.3	PF	F_C= 1 MHz
$C_{I/O2}$	I/O Capacitance	3.5	7.0	PF	F_C= 1 MHz
C_L	Crystal Load Capacitance	7.5	15	pF	

NOTES:
1. Refer to Table 2 for the signals associated with this specification.
2. V_{OL2} assumes R_L of 1.5 kΩ to 3.6V and V_{OH2} assumes R_L of 15 kΩ to GND.
3. During transitions, the inputs may overshoot beyond max V_{CC} or undershoot below V_{SS} by 0.8V for 7.0 ns on the 440MX inputs, with a maximum instantaneous overshoot/undershoot of ± 1.6V.
4. During transitions, the inputs may overshoot/undershoot beyond V_{TTmax} or below V_{SS} by ± 0.3V (violating the overshoot/undershoot guideline is acceptable, although satisfying the ringback specification will be very difficult as a result). Maximum rising edge ringback is 1.12V. Maximum falling edge ringback is 0.88V.
5. Parameter correlated into a 120 Ω resistor.
6. For 0.25µ Mobile Pentium II and Celeron processor designs.
7. For 0.18µ Mobile Pentium III and Celeron processor designs.

Table 2. DC Characteristic Signal Association (Sheet 1 of 2)

Symbol	Associated Signals
V_{IL1}/V_{IH1}	PWROK, RSMRST#, RTCX1/X2, TEST#, BATLOW#, EXSMI#, GPIO[0, 1, 4, 6, 9, 10, 11, 12, 17, 18, 20, 24], IRQ8#, LID, RI#, PWRBTN#, USBPRT[1:0]+, USBPRT[1:0]-, PME#, OC[1:0]#, IRQ14
V_{IL2}/V_{IH2}	SMBCLK, SMBDATA
V_{IL3}/V_{IH3}	PHLDA#, IOCHRDY, SD[7:0], ZEROWS#, A20GATE, RCIN#, DREQ[0:3], REQA#, IRQ[1, 3:7,12], PIRQ[A:D]#, SERIRQ, CLK48, PCICLK, OSC, PDD[15:0], PDDREQ, PIORDY, GPIO[5, 7, 13:16, 19, 21:23, 25:28]
V_{IL4}/V_{IH4}	MD[63:0], AD[31:0], DEVSEL#, FRAME#, IRDY#, C/BE[3:0]#, PAR, PLOCK#, TRDY#, STOP#, PREQ[2:0]#, PREQ3#/GPIO29, GPIO(8), FERR#, GPIO[30], DCLK. (HCLKIN is V_{IL4} only)
V_{IL5}/V_{IH5}	HA[31:3]#, HD[63:0]#, ADS#, DBSY#, DRDY#, HIT#, HITM#, HREQ[4:0]#, HTRDY#, RS[2:0]#, HLOCK#
V_{IL6}/V_{IH6}	CLKRUN#, SERR#
V_{IL7}/V_{IH7}	**AC'97 Signals:** AC_BITCLK, AC_SDATA_IN[1:0]
V_{OL1}/V_{OH1}	PDA[2:0], PDCS1#, PDCS3#, PDD[15:0], PDDACK#, PDIOR#, PDIOW#, CPUSTP#, EXSMI#, GPIO8, PCISTP#, SMBCLK, SMBDATA, SUS[A:C]#, SUS_STAT#, A20M#, CPURST, IGNNE#, INIT, INTR, NMI, SMI#, STPCLK#, BIOSCS#, KBCCS#, MCCS#, PCS0#, PCS1#, SUSCLK, RTCX2, SMBCLK, SMBDATA, IRQ[8], SPKR, GNTA#, SERIRQ, GPIO[0:26]

Table 2. DC Characteristic Signal Association (Sheet 2 of 2)

V_{OL2}/V_{OH2}	USBP[1:0]+, USBP[1:0]-
V_{OL3}/V_{OH3}	**X-Bus Output Signals:** IOR#, IOW#, MEMR#, MEMW#, RSTDRV, SA[18:0], SD[7:0], SYSCLK, DACK[0:3]#, TC **Other Signals:** GPIO[27, 28]
V_{OL4}/V_{OH4}	CS[3:0]#, CKE[3:0]#, DQM[7:0], SRAS#, SCAS#, MA13, MA[12:11,9:0]#, MA10, WE#, MD[63:0], DCLKO, PGNT[2:0]#, PGNT3#/GPIO30, AD[31:0], DEVSEL#, FRAME#, IRDY#, C/BE[3:0]#, PAR, PLOCK#, TRDY#, STOP#, PREQ[3:0]#, PCIRST#, GPIO[29]
V_{OL5}	HA[31:3]#, HD[63:0]#, ADS#, BNR#, DBSY#, DRDY#, HIT#, HITM#, HREQ[4:0]#, HTRDY#, RS[2:0]#, CPURST#, BPRI#, DEFER#, BREQ0#
V_{OL6}	CLKRUN#, SERR#
V_{OL7}/V_{OH7}	**AC'97 Signals:** AC_SYNC, AC_RST#, AC_SDATA_OUT
GTL_REF	GTL_REF
V_{TT}	$V_{TT[B:A]}$
$REFV_{CC}$	$REFV_{CC}$
I_{OL1}/I_{OH1}	**IDE Output Signals:** PDA[2:0], PDCS1#, PDCS3#, PDD[15:0], PDDAK#, PDIOR#, PDIOW#
I_{OL2}/I_{OH2}	**X-Bus Output Signals:** IOR#, IOW#, MEMR#, MEMW#, RSTDRV, SA[18:0], SD[7:0], SYSCLK, DACK[0:3]#, TC **Other Signals:** GPIO[27, 28]
I_{OL3}/I_{OH3}	**Power Management Signals:** CPUSTP#, EXSMI#, THRM#, PCISTP#, SMBCLK, SMBDATA, SUS[A:C]#, SUS_STAT# **CPU Interface Signals:** A20M#, CPURST#, IGNNE#, INTR, NMI **X-Bus Interface Signals:** BIOSCS#, KBCCS#, MCCS#, PCS0#, PCS1# **Other Signals:** SMBCLK, SMBDATA, IRQ8#, SPKR, GNTA#, GPIO[0:26], SUSCLK, CS[3:0]#, CKE[3:0]#, DQM[7:0], SRAS#, SCAS#, MA13, MA[12:11, 9:0]#, MA10, WE#, SUSCLK, SUS_STAT#, MD[63:0], DCLKO, PGNT[2:0]#, PGNT3#/GPIO30, AD[31:0], DEVSEL#, FRAME#, IRDY#, C/BE[3:0]#, PAR, PLOCK#, TRDY#, STOP#, PCIRST#, GPIO[29], RTCX2
I_{OL4}/I_{OH4}	**PCI Bus Signals:** AD[31:0], C/BE[3:0]#, CLKRUN#, DEVSEL#, FRAME#, IRDY#, PAR, PCIRST#, SERR#, STOP#, TRDY#, SERIRQ, SMI#, STPCLK#
I_{OL5}/I_{OH5}	**USB Signals:** USBPRT[1:0]+, USBPRT[1:0]-
I_{OL6}/I_{OH6}	INIT#
I_{OL7}	HA[31:3]#, HD[63:0]#, ADS#, BNR#, DBSY#, DRDY#, HIT#, HITM#, HREQ[4:0]#, HTRDY#, RS[2:0]#, BPRI#, DEFER#, BREQ0#
I_{OL8}/I_{OH8}	**AC'97 Signals:** AC_SYNC, AC_RST#, AC_SDATA_OUT
I_{IL1}/I_{IH1}	PCICLK, PREQ[2:0]#, PREQ3#/GPIO29, AD[31:0], DEVSEL#, FRAME#, IRDY#, C/BE[3:0]#, PAR, PLOCK#, TRDY#, STOP#, DCLKWR
C_{IN1}	PREQ[2:0]#, PREQ3#/GPIO29
C_{IN4}	CS[3:0]#, CKE[3:0]#, DQM[7:0], SRAS#, SCAS#, MA13, MA[12:11,9:0]#, MA10, WE#, MD[63:0]
C_{OUT1}	CS[3:0]#, CKE[3:0]#, DQM[7:0], SRAS#, SCAS#, MA13, MA[12:11,9:0]#, MA10, WE#, MD[63:0]
$C_{I/O1}$	AD[31:0], DEVSEL#, FRAME#, IRDY#, C/BE[3:0]#, PAR, PLOCK#, TRDY#, STOP#
$C_{I/O2}$	HA[31:3]#, HD[63:0]#, ADS#, BNR#, DBSY#, DRDY#, HIT#, HITM#, HREQ[4:0]#, HTRDY#, RS[2:0]#

Table 3. DC Current Characteristics

Functional Operating Range ($REFV_{CC}$ =5 V ± 5%, V_{CC} =3.3 V ± 5%, T_{CASE} = 0º C to +95º C)

Symbol	Parameter	Typ	Max	Unit	Notes
$I_{CC(3V)}$	V_{CC} Supply Current	500	1145	mA	Note 1, 2
$I_{CC(SUS)}$ ON	Suspend Well Supply Current: Full On	15	20	mA	Note 1, 2
$I_{CC(SUS)}$ POS/STR	Suspend Well Supply Current: Power-On Suspend or Suspend-to-RAM	0.5	1.1	mA	Note 1, 2
$I_{CC(SUS)}$ POS/STR	Suspend Well Supply Current: Power-On Suspend or Suspend-to-RAM	1.1	1.8	mA	Measured with USB buffers on Note 2
$I_{CC(SUS)}$ STD/Soff	Suspend Well Supply Current: Suspend-to-Disk or Soft Off	0.8	1.1	mA	Note 1, 2
$I_{CC(SUS)}$ STD/Soff	Suspend Well Supply Current: Suspend-to-Disk or Soft Off	1.4	1.8	mA	Measured with USB buffers on Note 2
$I_{CC(RTC)}$	Battery Standby Current	5	10	µA	$V_{CC(RTC)}$=3.0V Mech Off State Note 3

NOTES:
1. Not 100% tested. Specified by design characterization.
2. Typical value measured at 35° C. Maximum value measured at 95° C.
3. Typical value measured at 35° C. Maximum value measured at 50° C.

2.2 AC Characteristics

2.2.1 AC Characteristics Tables

All timings are in nanoseconds (ns), unless otherwise specified. In addition, all the clock-to-output values are specified into 0 pF load, unless otherwise specified.

Table 4. AC Timings for HCLKIN, DCLKO, and DCLK

Sym	Parameter	440MX 66 MHz		440MX 100 MHz		Unit	Figure	Notes
		Min	Max	Min	Max			
HCLKIN								
t1a	HCLKIN Period	15	15.5	10.0	10.5	ns	Figure 2	
t1b	HCLKIN Period Stability		± 300		± 250	ps		
t1c	HCLKIN High Time	5.3		3.1		ns	Figure 2	Measured @ 1.7V
t1d	HCLKIN Low Time	5.3		2.8		ns	Figure 2	Measured @ 0.7V
t1e	HCLKIN Rise Time	0.25	1.25	0.25	1.0	ns	Figure 2	0.7V -1.7V note 1
t1f	HCLKIN Fall Time	0.25	1.25	0.25	1.0	ns	Figure 2	1.7V - 0.7V note 1
DCLKO								
t2a	DCLKO Period	15	15.5	10	10.5	ns	Figure 4	
t2b	DCLKO Period Stability		± 350		± 350	ps		
t2c	DCLKO High Time	7.1		4.6		ns	Figure 4	
t2d	DCLKO Low Time	6.8		4.2		ns	Figure 4	
t2e	DCLKO Slew Rate	2	6	2	6	V/ns	Figure 4	
DCLK								
t3a	DCLK Period	15	15.5	10	10.5	ns	Figure 4	
t3b	DCLK Period Stability		± 550		± 550	ps		
t3c	DCLK High Time	6.0		3.0		ns	Figure 4	
t3d	DCLK Low Time	6.0		3.0		ns	Figure 4	
t3e	DCLK Slew Rate	0.8	4.0	0.8	4.0	V/ns	Figure 4	
t3f	DCLK Duty Cycle	40%	60%	40%	60%		Figure 5	

Table 5. AC Clock Timings for PCI, X-Bus, Oscillator, USB, Suspend, SMBus, and AC'97 (Sheet 1 of 2)

Functional Operating Range ($REFV_{CC}$ =5 V ± 5%, V_{CC} =3.3 V ± 5%, T_{CASE}=0° C to +95° C)

Sym	Parameter[1]	Min	Max	Unit	Figure	Notes
PCI Clock Timings (PCICLK)						
tc4a	Period	30	33.3	ns	Figure 3	
tc4b	High Time	12.0		ns	Figure 3	
tc4c	Low Time	12.0		ns	Figure 3	
tc4d	Rise Time		3.0	ns	Figure 3	
tc4e	Fall Time		3.0	ns	Figure 3	
tc4f	PCICLK Cycle to Cycle Jitter		500	ps		
tc4g	HCLKIN Lead Time to PCICLK	1.5	5	ns		
X-Bus Clock Timings (SYSCLK)						
tc5a	Period	120	133.3	ns	Figure 3	
tc5b	High Time	49		ns	Figure 3	
tc5c	Low Time	49		ns	Figure 3	
tc5d	Rise Time		4	ns	Figure 3	
tc5e	Fall Time		4	ns	Figure 3	
Oscillator Clock Timings (OSC)						
tc6a	OSC Period	67	70	ns	Figure 3	
tc6b	High Time	20			Figure 3	
tc6c	Low Time	20		ns	Figure 3	
USB Clock Timings						
tc7a	Operating Frequency	48		MHz		Frequency Tolerance ±2500 ppm[2]
tc7b	High Time	7		ns		
tc7c	Low Time	7		ns		
tc7d	Rise Time		1.2	ns		
tc7e	Fall Time		1.2	ns		
Suspend Clock Timings						
tc8a	SUSCLK Operating Frequency	32	KHz			
tc8b	High Time	10		µs		
tc8c	Low Time	10		µs		
SMBus Clock						
Tc9a	SMBCLK Operating Frequency	10	16	KHz		
Tc9b	High Time	4.0	50	µs	Figure 29	

NOTES:
1. AC specifications are measured at the 440MX.
2. Not 100% tested. Specified by design characterization as a clock driver requirement.

Table 5. AC Clock Timings for PCI, X-Bus, Oscillator, USB, Suspend, SMBus, and AC'97 (Sheet 2 of 2)

Functional Operating Range (REFV$_{CC}$ =5 V ± 5%, V$_{CC}$ =3.3 V ± 5%, T$_{CASE}$=0° C to +95° C)

Sym	Parameter[1]	Min	Max	Unit	Figure	Notes
Tc9c	Low Time	4.7		µs	Figure 29	
Tc9d	Clock/Data Rise Time		1000	ns	Figure 29	
Tc9e	Clock/Data Fall Time		300	ns	Figure 29	
AC'97 Clock						
Tc10a	Bit_CLK output jitter		750	ps		
Tc10b	Bit_CLK high pulse width	32.56	48.4	ns		
Tc10c	Bit_CLK low pulse width	32.56	48.4	ns		
Tc10d	Bit_CLK rise time	2.0	6.0	ns		
Tc10e	Bit_CLK fall time	2.0	6.0	ns		

NOTES:
1. AC specifications are measured at the 440MX.
2. Not 100% tested. Specified by design characterization as a clock driver requirement.

Table 6. AC'97 Timings

Functional Operating Range (V$_{TT}$ = 1.5 V ± 9%, V$_{CC}$ = 3.3 V ± 5%; T$_{CASE}$ = 0° C to +95° C)

Sym	Parameter	Min	Max	Unit	Figure	Notes
t1	SDATA_IN/SYNC setup to falling edge of BIT_CLK	10		ns		
t2	SDATA_IN/SYNC hold from falling edge of BIT_CLK	10		ns		
t3	SDATA_OUT/SYNC valid delay from rising edge of BIT_CLK		12	ns		
t4	SDATA_OUT/SYNC valid delay from falling edge of BIT_CLK	15		ns		

Table 7. Processor Interface Timing

Functional Operating Range (V$_{TT}$ = 1.5 V ± 9%, V$_{CC}$ = 3.3 V ± 5%; T$_{CASE}$[4] = 0° C to +95° C)

Sym	Parameter	440MX 66 MHz		440MX 100 MHz		Unit	Figure	Notes
		Min	Max	Min	Max			
t7	Valid Delay from HCLKIN Rising (tco)	1.10	10	1.2	4.45	ns		1, 2, 3
t8	Input Setup Time to HCLKIN Rising (tsu)	3.0		3.0		ns	Figure 6	1, 2
t9	Input Hold Time from HCLKIN Rising (thld)	-100		-100		ps	Figure 6	

NOTES:
1. 440MX 66 MHz valid delays are specified into a 120 Ω resistor which is tied to V$_{TT}$ = 1.7 V.
2. 440MX 100 MHz valid delays are specified into a 25 Ω resistor which is tied to V$_{TT}$ = 1.5 V.
3. Tco change made to support Ultra Low Voltage Pentium® III processor core voltage at 0.975 V.
4. T$_{CASE}$ = 0° C to +95° C is specified without a heat sink.

Table 8. 440MX 66 MHz SDRAM Memory Interface Timing (Sheet 1 of 2)

Functional Operating Range (V_{TT} = 1.5 V ± 9%, V_{CC} = 3.3 V ± 5%; T_{CASE} = 0° C to +95° C)

Sym	Parameter	1x Buffer		2x Buffer		3x Buffer		Figure	Notes
		Min	Max	Min	Max	Min	Max		
t10	WE# Valid Delay from DCLK (for the first chip select)	1.61 1.54	17.98 18.13	1.61 1.55	17.95 18.07	1.61 1.55	17.93 18.04	Figure 6	Rising Falling 1,2,3,4
t11	WE# Valid Delay from DCLK Rising (for the subsequent chip selects)	1.61 1.54	8.18 8.33	1.61 1.55	8.15 8.27	1.61 1.55	8.14 8.24	Figure 6	Rising Falling 1,2,3,4
t12	MA[12:11,9:0]#, MA10 Valid Delay from DCLK (first chip select of an access)	1.61 1.54	17.98 18.13	1.61 1.55	17.95 18.07	1.61 1.55	17.93 18.04	Figure 6	Rising Falling 1,2,3,4
t13	MA[12:11,9:0]#, MA10 Valid Delay from DCLK Rising, Read/Write cycles (for the subsequent chip selects)	1.61 1.54	8.18 8.33	1.61 1.55	8.15 8.27	1.61 1.55	8.14 8.24	Figure 6	Rising Falling 1,2,3,4
t14	SRAS# Valid Delay from DCLK (first chip select of an access)	1.61 1.54	17.98 18.13	1.61 1.55	17.95 18.07	1.61 1.55	17.93 18.04	Figure 6	Rising Falling 1,2,3,4
t15	SRAS# Valid Delay from DCLK Rising (subsequent chip selects)	1.61 1.54	8.18 8.33	1.61 1.55	8.15 8.27	1.61 1.55	8.14 8.24	Figure 6	Rising Falling 1,2,3,4
t16	SCAS# Valid Delay from DCLK (for the first chip select)	1.61 1.54	17.98 18.13	1.61 1.55	17.95 18.07	1.61 1.55	17.93 18.04	Figure 6	Rising Falling 1,2,3,4
t17	SCAS# Valid Delay from DCLK Rising (subsequent chip selects)	1.61 1.54	8.18 8.33	1.61 1.55	8.15 8.27	1.61 1.55	8.14 8.24	Figure 6	Rising Falling 1,2,3,4
t18	CS[3:0]# Valid Delay from DCLK Rising	1.72 1.56	5.87 5.54	1.56 1.56	5.85 5.67	N/A	N/A	Figure 6	Rising Falling 1,2,3,4
t19	CKE[3:0]# Valid Delay from DCLK Rising	1.53 1.65	5.59 6.2	1.53 1.63	5.63 6.07	1.54 1.62	5.64 6.2	Figure 6	Rising Falling 1,2,3,4
t20	DQM[7:0] Valid Delay from DCLK Rising	1.57 1.70	5.78 5.74	1.51 1.61	5.69 5.63	1.51 1.59	5.63 5.63	Figure 6	Rising Falling 1,2,3,4

NOTES:
1. Two valid delays apply to these command signals. The longer valid delay applies to command signals set-up to the first chip select of an access. The second valid delay applies command signals set-up to subsequent chip selects in the access. However, in a pipe-lined access, the shorter valid delay applies to command signals set-up to the first chip select.
2. All measurements are in ns, unless otherwise specified.
3. The choice of 66 MHz buffers is independent of bus frequency. It is possible to select a 100 MHz memory buffer even though the bus frequency is 66 MHz depending on memory signal integrity analysis.
4. Applies to rising and falling edges.

Table 8. 440MX 66 MHz SDRAM Memory Interface Timing (Sheet 2 of 2)

Functional Operating Range (V_{TT} = 1.5 V ± 9%, V_{CC} = 3.3 V ± 5%; T_{CASE} = 0° C to +95° C)

Sym	Parameter	1x Buffer		2x Buffer		3x Buffer		Figure	Notes
		Min	Max	Min	Max	Min	Max		
t22	MD[63:0] Valid Delay from DCLK Rising	1.59 1.73	5.54 5.75	1.58 1.63	5.56 5.65	N/A	N/A	Figure 6	Rising Falling 1,2,3,4
t23	MD[63:0] Setup Time to DCLK Rising	0.47		0.47		0.47		Figure 6	1,2,3,4
t24	MD[63:0] Hold Time from DCLK Rising	1.5		1.5		1.5		Figure 6	1,2,3,4

NOTES:
1. Two valid delays apply to these command signals. The longer valid delay applies to command signals set-up to the first chip select of an access. The second valid delay applies command signals set-up to subsequent chip selects in the access. However, in a pipe-lined access, the shorter valid delay applies to command signals set-up to the first chip select.
2. All measurements are in ns, unless otherwise specified.
3. The choice of 66 MHz buffers is independent of bus frequency. It is possible to select a 100 MHz memory buffer even though the bus frequency is 66 MHz depending on memory signal integrity analysis.
4. Applies to rising and falling edges.

Table 9. 440MX 100 MHz Memory Interface Timing

Functional Operating Range (V_{CC} = 3.3 V ± 5%; T_{CASE} = 0° C to +95° C[5], C_L = 0 pF)

Sym	Parameter	1x Buffer		2x Buffer		3x Buffer		Figure	Notes
		Min	Max	Min	Max	Min	Max		
t10a	WE# Valid Delay from DCLK (for the first chip select)	1.25	18.31	1.19	18.18	1.19	18.13	Figure 6	1,2,3,4
t11a	WE# Valid Delay from DCLK Rising (for the subsequent chip selects)	1.25	8.51	1.19	8.38	1.19	8.33	Figure 6	1,2,3,4
t12a	MA[12:11,9:0]#, MA10 Valid Delay from DCLK (first chip select of an access)	1.25	18.31	1.19	18.18	1.50	18.13	Figure 6	1,2,3,4
t13a	MA[12:11,9:0]#, MA10 Valid Delay from DCLK Rising, Read/Write cycles (for the subsequent chip selects)	1.25	8.51	1.19	8.38	1.9	8.33	Figure 6	1,2,3,4
t14a	SRAS# Valid Delay from DCLK (first chip select of an access)	1.25	18.31	1.19	18.18	1.50	18.13	Figure 6	1,2,3,4
t15a	SRAS# Valid Delay from DCLK Rising (subsequent chip selects)	1.25	8.51	1.19	8.38	1.9	8.33	Figure 6	1,2,3,4
t16a	SCAS# Valid Delay from DCLK (for the first chip select)	1.25	18.31	1.19	18.18	1.50	18.13	Figure 6	1,2,3,4
t17a	SCAS# Valid Delay from DCLK Rising (subsequent chip selects)	1.25	8.51	1.19	8.38	1.9	8.33	Figure 6	1,2,3,4
t18a	CS[3:0]# Valid Delay from DCLK Rising	1.08 1.13	4.15 3.88	0.90 1.05	2.80 3.50	N/A N/A	N/A N/A	Figure 6	Rising Falling
t19a	CKE[3:0]# Valid Delay from DCLK Rising	1.04 1.07	3.87 3.76	0.90 1.03	3.55 3.68	0.87 1.03	3.11 3.46	Figure 6	Rising Falling
t20a	DQM[7:0] Valid Delay from DCLK Rising	1.12 1.13	3.87 3.61	0.92 1.14	2.80 2.80	0.83 0.93	3.11 3.52	Figure 6	Rising Falling
t22a	MD[63:0] Valid Delay from DCLK Rising	1.17 1.14	3.20 3.20	0.96 0.93	2.70 2.70	0.88 0.83	2.50 3.25	Figure 6	Rising Falling
t23a	MD[63:0] Setup Time to DCLK Rising	0.47		0.47		0.6 0.47		Figure 6	2,4
t24a	MD[63:0] Hold Time from DCLK Rising	1.5		1.5		1.5		Figure 6	2,4

NOTES:

1. Two valid delays apply to these command signals. The longer valid delay applies to command signals set-up to the first chip select of an access. The second valid delay applies command signals set-up to subsequent chip selects in the access. However, in a pipelined access, the shorter valid delay applies to command signals set-up to the first chip select.
2. All measurements are in ns, unless otherwise specified.
3. The choice of 100 MHz or 66 MHz buffers is independent of bus frequency. It is possible to select a 100 MHz memory buffer even though the bus frequency is 66 MHz (and vice versa) depending on memory signal integrity analysis.
4. Applies to rising and falling edges.
5. T_{CASE} = 0º C to +95º C is specified without a heat sink.

Table 10. PCI Interface Timing, 33 MHz

Functional Operating Range (V_{CC} = 3.3 V ± 5%; T_{CASE} = 0º C to +95º C[1])

Sym	Parameter	Min	Max	Unit	Figure	Notes
t37	AD[31:0] Valid Delay from PCICLK Rising	2	11	ns		Min: 0 pF Max: 50 pF
t38	AD[31:0] Setup Time to PCICLK Rising	7		ns	Figure 6	
t39	AD[31:0] Hold Time from PCICLK	0		ns	Figure 6	
t40	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, DEVSEL#, SERR#, Valid Delay from PCICLK Rising	2	11	ns		Min: 0 pF Max: 50 pF
t41	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, DEVSEL#, SERR#, Output Enable Delay from PCICLK Rising	2	11	ns		
t42	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, DEVSEL#, SERR#, Float Delay from PCICLK Rising	2	28	ns	Figure 6	
t43	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, DEVSEL#, SERR#, Setup Time to PCICLK Rising	7		ns	Figure 6	
t44	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, DEVSEL#, SERR#, Hold Time from PCICLK Rising	0		ns	Figure 6	
t48	PGNT[2:0]#, GNT3#/GPIO30 Valid Delay from PCICLK Rising	2	12	ns		Min: 0 pF Max: 50 pF
t49	PREQ[2:0]#, PREQ3#/GPIO29 Setup Time to PCICLK Rising	12		ns	Figure 6	
t50	PREQ[2:0]#, PREQ3#/GPIO29 Hold Time from PCICLK Rising	0		ns	Figure 6	
t51	PCIRST# Low Pulse Width	1		ms	Figure 6	

NOTE:
1. T_{CASE} = 0º C to +95º C is specified without a heat sink.

Table 11. VTclock and VTsignal Reference Points

Signal Group	VTclock	VTsignal
GTL	1.25V	1.0V
DRAM	1.4V	1.4V
PCI (3.3V)	1.5V	0.285 V_{CC} (R) 0.615 V_{CC} (F)

Table 12. TT_ClkResetTimReset Timings

Functional Operating Range (REFV_{CC} =5 V ± 5%, V_{CC} =3.3 V ± 5%, T_{CASE} =0° C to +95° C)

Sym	Parameter	Min	Max	Unit	Figure	Notes
Reset Timings						
t2f	PCIRST#, RSTDRV Driven Inactive After SUS_STAT# is Driven Inactive.		1	RTCCLK	Figure 7	
t2g	CPURST#, PCIRST#, RSTDRV Active Pulse Width. Initiated via the RC Register.	1		ms	Figure 8	
t2h	CPURST# Driven Inactive After PCIRST# is Driven Inactive.		1	ms	Figure 7	
t2i	CPURST# Valid Delay from HCLK Rising	2	25	ns		
t2j	PWROK, RSMRST# Rise Time		10	ns		1
SMI#						
t3a	Valid Delay from PCICLK	2	25	ns	Figure 11	
t3b	Active Pulse Width	3		PCICLK	Figure 9	
t3c	Inactive Pulse Width	4		PCICLK	Figure 9	
EXSMI#						
t3d	Active Pulse Width	2		PCICLK	Figure 9	
t3e	Inactive Pulse Width	4		PCICLK	Figure 9	
t3f	Valid Setup to PCICLK	10		ns	Figure 10	
t3g	Valid Hold from PCICLK	4		ns	Figure 10	
STPCLK#						
t3h	Valid Delay from PCICLK	2	25	ns	Figure 11	
t3i	STPCLK# Inactive Pulse Width	5		PCICLK	Figure 9	

NOTE:
1. t2j is measured as a transition time through the threshold region VOL = 0.8 V and VOH = 2.0 V.

Table 13. X-Bus Timings (Sheet 1 of 5)

Functional Operating Range (REFV$_{CC}$ =5 V ± 5%, V$_{CC}$ =3.3 V ± 5%, T$_{CASE}$ = 0° C to +95° C)

Sym	Parameter	Min	Max	Units	Type	Size	Figure	Notes
440MX as Master Timings								
SA[18:0]								
t6c	SA[18:0] Setup to MEMx#, IOx# Active	100		ns	M,I/O	8	Figure 12, Figure 13	
t6e	SA[18:0] Valid Hold from MEMx#, IOx# Inactive	41		ns	M,I/O	8	Figure 12, Figure 13	
MEMR#, MEMW#, IOR# and IOW#								
t7d	MEMx# or IOx# Active Pulse Width (std)	520		ns	M,I/O	8	Figure 12, Figure 13	
t7e	MEMx# or IOx# Active Pulse Width (nws)	160		ns	M,I/O	8	Figure 12, Figure 13	1
t7g	MEMx# Inactive Pulse Width	163		ns	M	8	Figure 12	
t7h	IOx# Inactive Pulse Width	163		ns	I/O	8	Figure 13	
t7i	MEMx#, IOx# Driven Inactive from IOCHRDY Active	120		ns	M,I/O	8	Figure 12, Figure 13	
Read Data								
t9a	Read Data Driven from MEMR#, IOR# Active	0		ns	M,I/O	8	Figure 12, Figure 13	
t9b	Read Data Valid Setup to MEMR#, IOR# Inactive	24		ns	M,I/O	8	Figure 12, Figure 13	
t9c	Read Data Valid Hold from MEMR#, IOR# Inactive	0		ns	M,I/O	8	Figure 12, Figure 13	
t9d	Read Data Three-stated from MEMR# and IOR# Inactive		41	ns	M,I/O	8	Figure 12, Figure 13	
Write Data								
t10a	Write Data Valid Setup to MEMW# Active Write Data Valid Setup to IOW# Active	-40 -40		ns ns	M,I/O M,I/O	8 8	Figure 12, Figure 13	
t10b	Write Data Valid Hold from MEMW#, IOW# Inactive	45		ns	M,I/O	8	Figure 12, Figure 13	
t10c	Write Data Three-stated from MEMW#, IOW# Inactive		105	ns	M,I/O	8	Figure 12, Figure 13	
t10d	Write Data Driven Valid after Read MEMR#, IOR# Inactive	41		ns	M,I/O	8	Figure 12, Figure 13	

NOTES:
1. No-wait-state (ZEROWS#) asserted.
2. This applies to the last cycle of a demand mode DMA transfer.
3. Output from the 440MX.
4. 440MX as a master cycle only.
5. Type F transfers are selected via the MBDMAX register.

Table 13. X-Bus Timings (Sheet 2 of 5)

Functional Operating Range ($REFV_{CC}$ =5 V ± 5%, V_{CC} =3.3 V ± 5%, T_{CASE} = 0° C to +95° C)

Sym	Parameter	Min	Max	Units	Type	Size	Figure	Notes
ZEROWS#								
t13b	ZEROWS# Driven Active from MEMx#, IOx# Active		80	ns	M,I/O	8	Figure 12, Figure 13	
t13f	ZEROWS# Driven Active from SA[18:0] Valid		200	ns	M,I/O	8	Figure 12, Figure 13	
IOCHRDY								
t15b	IOCHRDY Driven Inactive from MEMx#, IOx# Active		366	ns	M,I/O	8	Figure 12, Figure 13	
t15e	IOCHRDY Inactive Pulse Width	0.12	15.6	µs	M,I/O	8	Figure 12, Figure 13	
Interrupt and NMI Timings								
NMI Timing								
t23a	SERR# Active to NMI Driven Active		200	ns			Figure 14	
Interrupt Timing								
t24a	IRQx Inactive Pulse Width	100		ns			Figure 15	
DMA Compatible Timings								
DREQ								
t30a	DREQ Active Hold from IOR# Active		558	ns			Figure 17	2
t30b	DREQ Active Hold from IOW# Active		315	ns			Figure 16	2
DACK#								
t31a	DACK# Active to IOR# Active	73		ns			Figure 17	
t31b	DACK# Active to IOW# Active	312		ns			Figure 16	
t31c	DACK# Active Hold from IOR# Inactive	100		ns			Figure 17	
t31d	DACK# Active Hold from IOW# Inactive	155		ns			Figure 16	
MEMR#, MEMW#, IOR#, IOW#								
t34a	IOW# and MEMW# Active Pulse Width	465		ns			Figure 16, Figure 17	
t34b	MEMR# Active Pulse Width	495		ns			Figure 16	
t34c	IOR# Active Pulse Width	760		ns			Figure 17	
t34d	IOW# Inactive Pulse Width (continuous)	465		ns			Figure 16	

NOTES:
1. No-wait-state (ZEROWS#) asserted.
2. This applies to the last cycle of a demand mode DMA transfer.
3. Output from the 440MX.
4. 440MX as a master cycle only.
5. Type F transfers are selected via the MBDMAX register.

Table 13. X-Bus Timings (Sheet 3 of 5)

Functional Operating Range ($REFV_{CC}$ =5 V ± 5%, V_{CC} =3.3 V ± 5%, T_{CASE} = 0° C to +95° C)

Sym	Parameter	Min	Max	Units	Type	Size	Figure	Notes
t34e	IOR# Inactive Pulse Width (continuous)	160		ns			Figure 17	
t34f	IOR# Active to MEMW# Active	230		ns				
t34g	MEMR# Active to IOW# Active	-26		ns				
t34h	MEMR# Active Hold from IOW# Inactive	40		ns				
t34i	IOR# Active Hold from MEMW# Inactive	40		ns				
t34j	MEMx# Active Hold from IOCHRDY Active	120		ns				
Read Data								
t36a	Read Data Valid from IOR# Active		237	ns			Figure 17	
t36b	Read Data Valid Hold from IOR# Inactive	0		ns			Figure 17	
t36c	Read Data Float from IOR# Inactive		61	ns			Figure 17	
Write Data								
t37a	Write Data Valid Setup to IOW# Inactive	225		ns			Figure 16	
t37b	Write Data Valid Hold from IOW# Inactive	36		ns			Figure 16	
TC								
t39a	TC Active Setup to IOx# Inactive	511		ns			Figure 16, Figure 17	3
t39b	TC Active Hold from IOx# Inactive	71		ns			Figure 16, Figure 17	3
t39h	TC Pulse Width	700		ns			Figure 16, Figure 17	
IOCHRDY								
t40c	IOCHRDY Inactive Pulse Width	125		ns			Figure 16, Figure 17	
DMA Type “F” Timings								
DREQ								
t55a	DREQ Active Hold from IOR# Active		82	ns			Figure 18	2, 5
t55b	DREQ Active Hold from IOW# Active		82	ns			Figure 18	2, 5

NOTES:
1. No-wait-state (ZEROWS#) asserted.
2. This applies to the last cycle of a demand mode DMA transfer.
3. Output from the 440MX.
4. 440MX as a master cycle only.
5. Type F transfers are selected via the MBDMAX register.

Table 13. X-Bus Timings (Sheet 4 of 5)

Functional Operating Range ($REFV_{CC}$ =5 V ± 5%, V_{CC} =3.3 V ± 5%, T_{CASE} = 0° C to +95° C)

Sym	Parameter	Min	Max	Units	Type	Size	Figure	Notes
DACK#								
t56a	DACK# Active to IOR# Active	77		ns			Figure 18	5
t56b	DACK# Active to IOW# Active	77		ns			Figure 18	5
t56c	DACK# Active Hold from IOR# Inactive	30		ns			Figure 18	5
t56d	DACK# Active Hold from IOW# Inactive	30		ns			Figure 18	5
IOR# and IOW#								
t58a	IOR# Active Pulse Width	110		ns			Figure 18	
t58b	IOW# Active Pulse Width	110		ns			Figure 18	
t58c	IOR# Inactive Pulse Width (Continuous)	115		ns			Figure 18	
t58d	IOW# Inactive Pulse Width (Continuous)	115		ns			Figure 18	
Read Data								
t59a	Read Data Valid from IOR# Active		96	ns			Figure 18	
t59b	Read Data Valid Hold from IOR# Inactive	2		ns			Figure 18	
t59c	Read Data Float from IOR# Inactive		61	ns			Figure 18	
Write Data								
t60a	Write Data Valid Setup to IOW# Inactive	70		ns			Figure 18	
t60b	Write Data Valid Hold from IOW# Inactive	31		ns			Figure 18	
TC								
t61a	TC Active Setup to IOR# Inactive	40		ns			Figure 18	6
t61b	TC Active Setup to IOW# Inactive	40		ns			Figure 18	6
t61c	TC Active Hold from IOx# Inactive	0		ns			Figure 18	6
440MX Accesses to the X-Bus								
BIOSCS#, KBCCS#, AND PCS0#, PCS1#, MCCS#								
t68a	CS# Driven Active from SA[18:0] Valid (except BIOSCS#)		35	ns			Figure 19	
t68b	CS# Driven Inactive from SA[18:0] Invalid (except BIOSCS#)		35	ns			Figure 19	

NOTES:
1. No-wait-state (ZEROWS#) asserted.
2. This applies to the last cycle of a demand mode DMA transfer.
3. Output from the 440MX.
4. 440MX as a master cycle only.
5. Type F transfers are selected via the MBDMAX register.

Table 13. X-Bus Timings (Sheet 5 of 5)

Functional Operating Range ($REFV_{CC}$ =5 V ± 5%, V_{CC} =3.3 V ± 5%, T_{CASE} = 0° C to +95° C)

Sym	Parameter	Min	Max	Units	Type	Size	Figure	Notes
t69b	BIOSCS# Active from IOx#, MEMx# Active		29	ns			Figure 19	
t69d	BIOSCS# Inactive from IOx#, MEMx# Inactive	35	120	ns			Figure 19	4
Miscellaneous X-Bus Timings								
Mouse Timing Support								
t71a	IRQ12/M and IRQ1 Minimum Active Pulse Width (for Mouse Function and Keyboard)	180		ns			Figure 20	
Coprocessor Error Support								
t73a	IGNNE# Active from IOW# Active from Port F0h Access		220	ns			Figure 20	
t73b	IGNNE# Inactive from FERR# Inactive		230	ns			Figure 20	
Speaker Timing								
t76a	SPKR Valid Delay from OSC Falling		200	ns			Figure 21	

NOTES:
1. No-wait-state (ZEROWS#) asserted.
2. This applies to the last cycle of a demand mode DMA transfer.
3. Output from the 440MX.
4. 440MX as a master cycle only.
5. Type F transfers are selected via the MBDMAX register.

Table 14. PCI Bus IDE Timing

Functional Operating Range (REFV_{CC} =5 V ± 5%, V_{CC} =3.3 V ± 5%, T_{CASE} = 0° C to +95° C)

Sym	Parameter	Min	Max	Unit	Figure	Notes
Primary IDE Timing						
t102	PDIOW# Active from PCICLK Rising	2	20	ns	Figure 24, Figure 25	
t103	PDIOW# Inactive from PCICLK Rising	2	20	ns	Figure 24, Figure 25	
t104	PDIOR# Active from PCICLK Rising	2	20	ns	Figure 24, Figure 25	
t105	PDIOR# Inactive from PCICLK Rising	2	20	ns	Figure 24, Figure 25	
t106	PDA[2:0] Valid Delay from PCICLK Rising	2	30	ns	Figure 24	
t107	PDCS1#, PDCS3# Active from PCICLK Rising	2	30	ns	Figure 24	
t108	PDCS1#, PDCS3# Inactive from PCICLK Rising	2	30	ns		
t113	PDDAK# Active from PCICLK Rising	2	20	ns	Figure 25	
t114	PDDAK# Inactive from PCICLK Rising	2	20	ns	Figure 25	
t114a	PDDRQ Setup Time to PCICLK Rising	7		ns	Figure 25	
t114b	PDDRQ Hold from PCICLK Rising	7		ns	Figure 25	
t115	PDD[15:0] Valid Delay from PCICLK Rising	2	30	ns	Figure 24, Figure 25	
t115a	PDD[15:0] Setup Time to PCICLK Rising	10		ns	Figure 24, Figure 25	
t115b	PDD[15:0] Hold from PCICLK Rising	8		ns	Figure 24, Figure 25	
t116	PIORDY Setup Time to PCICLK Rising	7		ns	Figure 24	1
t117	PIORDY Hold from PCICLK Rising	7		ns	Figure 24	1
t117a	PIORDY Inactive Pulse Width	48		ns	Figure 24	
t118	PIORDY Sample Point from PDIOx# Assertion			PCICLK	Figure 24	2,3
t119	PDIOx# Active Pulse Width			PCICLK	Figure 24, Figure 25	2,3
t120	PDIOx# Inactive Pulse Width			PCICLK	Figure 24, Figure 25	3,4

NOTES:
1. IORDY is internally synchronized. This timing is to guarantee recognition on the next clock.
2. This parameter is programmable from 2–5 PCI clocks when the drive mode is Mode 2 or greater. Refer to the ISP field in the IDE Timing Register.
3. The cycle time is the compatible timing when the drive mode is Mode 0/1. Refer to the TIM0/1 field in the IDE timing register.
4. This parameter is programmable from 1–4 PCI clocks when the drive mode is Mode 2 or greater. Refer to the RCT field in the IDE Timing Register.

Table 15. Universal Serial Bus Timing

Functional Operating Range (REFV$_{CC}$ =5 V ± 5%, V$_{CC}$ =3.3 V ± 5%, T$_{CASE}$ = 0° C to +95° C)

Sym	Parameter	Min	Max	Unit	Figure	Notes
	Full Speed Source (Note 7)					
t122	USBPRTx+, USBPRTx- Driver Rise Time	4	20	ns	Figure 26	1, CL=50 pF
t123	USBPRTx+, USBPRTx- Driver Fall Time	4	20	ns	Figure 26	1, CL=50 pF
t124a	Source Differential Driver Jitter: to Next Transition	-2	2	ns	Figure 27	2,3
t124b	Source Differential Driver Jitter: for Paired Transitions	-1	1	ns	Figure 27	2,3
t125	Source EOP Width	160	175	ns	Figure 28	4
t126	Differential to SE0 Transition Skew	-2	5	ns		5
t127a	Receiver Data Jitter Tolerance: to Next Transition	-20	20	ns	Figure 27	3
t127b	Receiver Data Jitter Tolerance: for Paired Transitions	-10	10	ns	Figure 27	3
t128a	EOP Width: Must reject as EOP	40		ns	Figure 28	4
t128b	EOP Width: Must accept as EOP	85		ns	Figure 28	4
	Low Speed Source (Note 8)					
t122	USBPRTx+, USBPRTx- Driver Rise Time	75	300	ns	Figure 26	1,6 CL =50 pF CL=350 pF
t123	USBPRTx+, USBPRTx- Driver Fall Time	75	300	ns	Figure 26	1,6 CL=50 pF CL=350 pF
t124a	Source Differential Driver Jitter: to Next Transition	-2	2	ns	Figure 27	2,3
t124b	Source Differential Driver Jitter: for Paired Transitions	-1	1	ns	Figure 27	2,3
t125	Source EOP Width	160	175	ns	Figure 28	4
t126	Differential to SE0 Transition Skew	-2	5	ns		5
t127a	Receiver Data Jitter Tolerance: to Next Transition	-20	20	ns	Figure 27	3
t127b	Receiver Data Jitter Tolerance: for Paired Transitions	-10	10	ns	Figure 27	3
t128a	EOP Width: Must reject as EOP	40		ns	Figure 28	4
t128b	EOP Width: Must accept as EOP	85		ns	Figure 28	4

NOTES:
1. Driver output resistance under steady state drive is specified at 28 Ω minimum and 43 Ω maximum.
2. Timing difference between the differential data signals.
3. Measured at crossover point of differential data signals.
4. Measured at 50% swing point of data signals.
5. Measured from last crossover point to 50% swing point of data line at leading edge of EOP.
6. Measured from 10% to 90% of the data signal.
7. Full Speed Data Rate has a minimum of 11.97 Mbps and a maximum of 12.03 Mbps.
8. Low Speed Data Rate has a minimum of 1.48 Mbps and a maximum of 1.52 Mbps.

Table 16. SMBus Timing

Functional Operating Range (REFV$_{CC}$ =5 V ± 5%, V$_{CC}$ =3.3 V ± 5%, T$_{CASE}$ = 0° C to +95° C)

Sym	Parameter	Min	Max	Unit	Figure	Notes
t141	Bus free time between Stop and Start Condition	4.7		µs	Figure 29	
t142	Hold time after (repeated) Start Condition. After this period, the first clock is generated	4.0		µs	Figure 29	
t143	Repeated Start Condition setup time	4.7		µs	Figure 29	
t144	Stop Condition setup time	4.0		µs	Figure 29	
t145	Data hold time	300		ns	Figure 29	
t146	Data setup time	250		ns	Figure 29	
t147	Device time out	25	35	ms		1
t148	Cumulative clock low extend time (slave device)		25	ms	Figure 30	2
t149	Cumulative clock low extend time (master device)		10	ms	Figure 30	3

NOTES:
1. A device will timeout when any clock low exceeds this value.
2. t148 is the cumulative time a slave device is allowed to extend the clock cycles in one message from the initial start to stop. If a slave device exceeds this time, it is expected to release both its clock and data lines and reset itself.
3. t149 is the cumulative time a master device is allowed to extend its clock cycles within each byte of a message as defined from start-to-ack, ack-to-ack, or ack-to-stop.

Table 17. Serial IRQ Timing

Functional Operating Range (REFV$_{CC}$ =5 V ± 5%, V$_{CC}$ =3.3 V ± 5%, T$_{CASE}$ = 0° C to +95° C)

Sym	Parameter	Min	Max	Unit	Figure	Notes
t151	SERIRQ Setup Time to PCICLK Rising	7		ns		
t152	SERIRQ Hold Time from PCICLK Rising	0		ns		

Table 18. Ultra DMA/33 Timing

Functional Operating Range (REFV$_{CC}$ =5 V ± 5%, V$_{CC}$ =3.3 V ± 5%, T$_{CASE}$ = 0° C to +95° C)

Sym	Parameter[1]	Mode 0		Mode 1		Mode 2		Unit	Figure
		Min	Max	Min	Max	Min	Max		
t154	Cycle Time (Tcyc)(2)	114		75		55		ns	Figure 32
t155	Two Cycle Time (T2cyc)	235		156		117		ns	Figure 32
t156	Data Setup Time (Tds)	15		10		7		ns	Figure 32
t157	Data Hold Time (Tdh)	5		5		5		ns	Figure 32
t158	Data Valid Setup Time (Tdvs)	70		48		34		ns	Figure 32
t159	Data Valid Hold Time (Tdvh)	6		6		6		ns	Figure 32
t160	Limited Interlock Time (Tli)	0	150	0	150	0	150	ns	Figure 34
t161	Interlock Time w/Minimum (Tmli)	20		20		20		ns	Figure 34
t162	Envelope Time (Tenv)	20	70	20	70	20	70	ns	Figure 31
t163	Ready to pause Time (Trp)	160		125		100		ns	Figure 33
t164	STOP, PDMARDY#, PDA[2:0], PDCS1#, and PDCS3#, setup/ hold Time to DMACK# (Tack)	20		20		20		ns	Figure 31, Figure 34

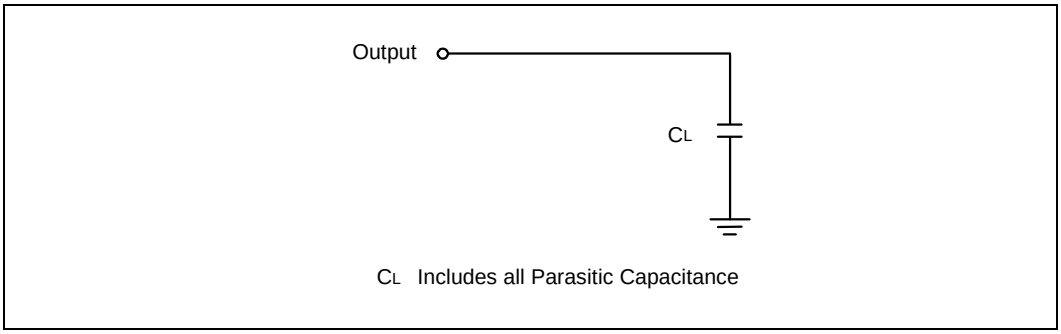
NOTES:
1. The specification symbols in parenthesis correspond to the Ultra DMA/33 specification name.
2. These cycle timings are based on the STROBE period as indicated in Figure 32. However, The *Intel® 440MX-100 PCIset* datasheet refers to cycle time strobe periods as 120 ns, 90 ns and 60 ns for mode 0, 1, and 2 respectively. The datasheet timings are different because they are based on the number of PCI clocks per cycle, not the actual period between the rise and fall of STROBE.

Table 19. AC Test Loads

Capacitive Load	Signals
120 pf	TC, SD[7:0], SA[18:0], MEMR#, MEMW#, IOR#, IOW#, IOCHRDY, ZEROWS#, RSTDRV, SYSCLK
50 pf	DACK#[7:5,3:0], SPKR, INTR, NMI, BIOSCS#, KBCCS#, PCS[1:0]#, MCCS#, IGNNE#, PDD[15:0], DIOR#, DIOW#, PDDAK#, PDCS1# PDCS3#, PDA[2:0]

2.2.2 AC Characteristic Figures

Figure 1. Test Load



2.2.3 Clock, Reset, ISA Bus, X-Bus and Host Timing Diagrams

Figure 2. 2.5 V Clocking Interface

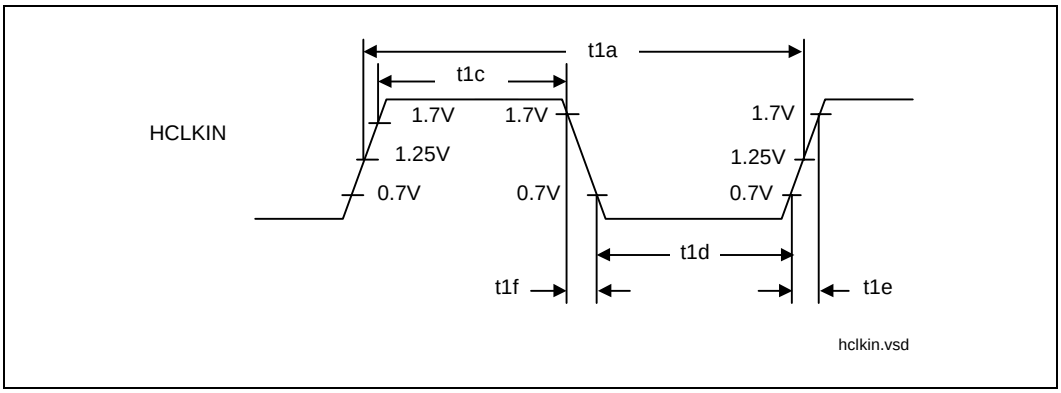


Figure 3. Clock Timing

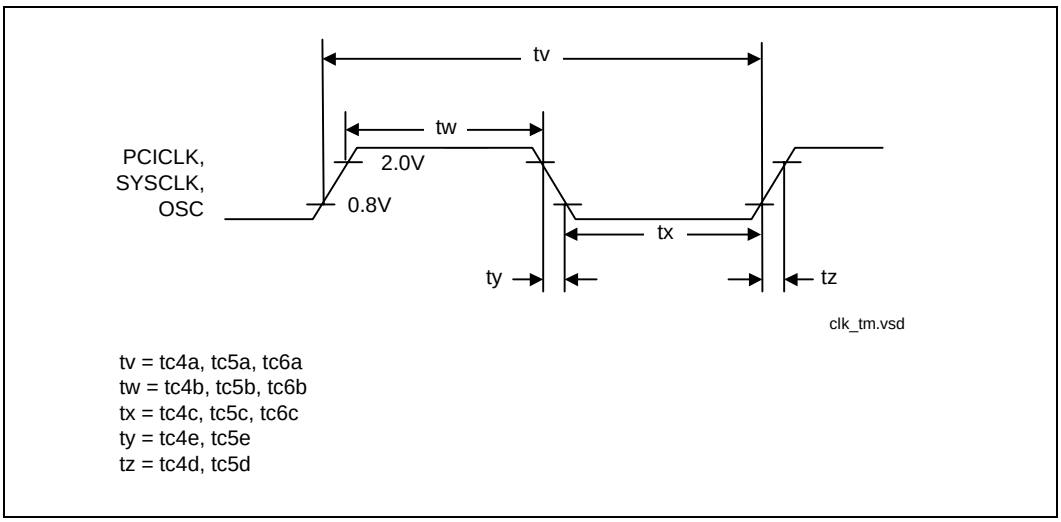


Figure 4. 3.3 V Clocking Interface

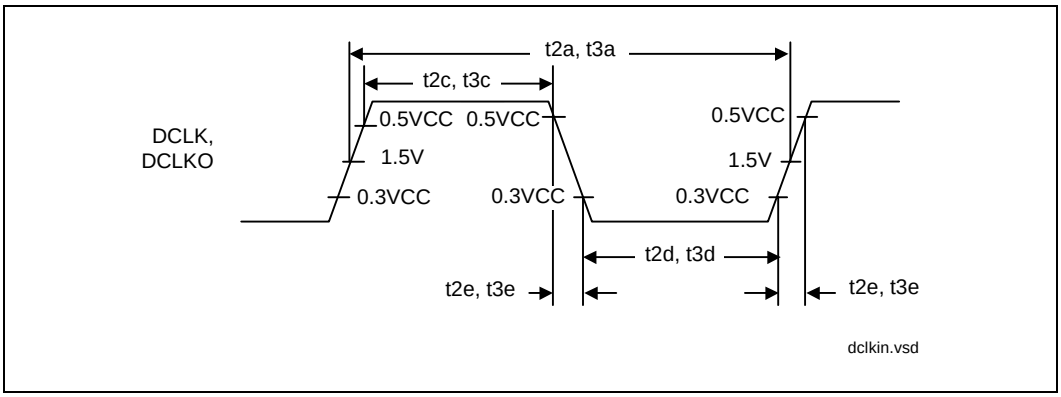
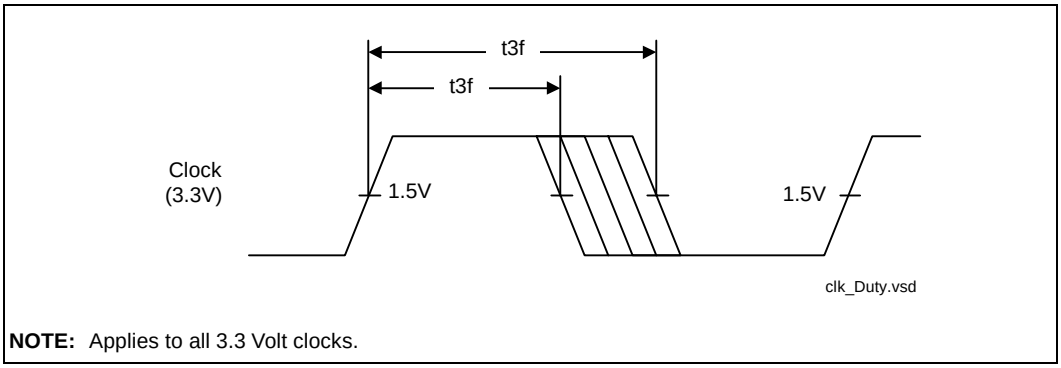
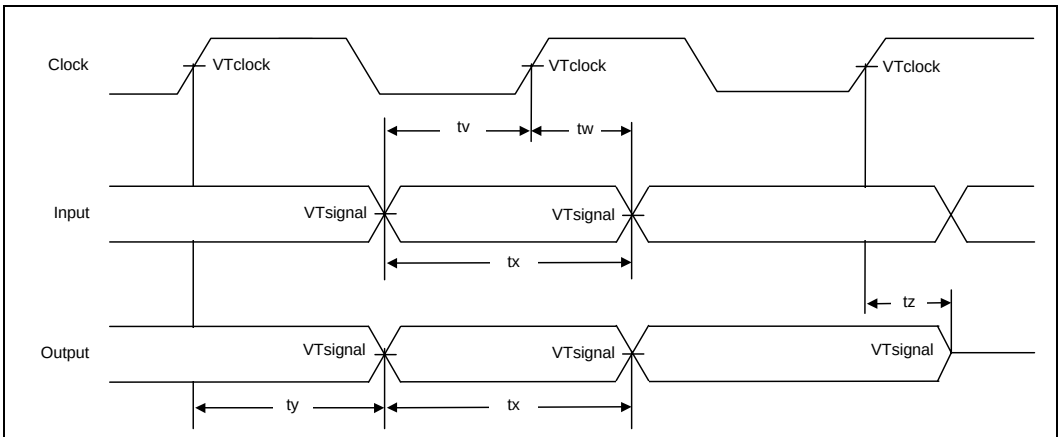


Figure 5. 3.3 V Clock Duty Cycle



NOTE: Applies to all 3.3 Volt clocks.

Figure 6. PCI Input/Output Timings



tv = t8, t23, t23a, t38, t49
tw = t9, t24, t24a, t39, t50
tx = t51
ty = t10a, t10, t11a, t11, t12a, t12, t13a, t13, t14a, t14, t15a, t15, t16a, t16, t17a, t17, t18a, t18, t19a, t19, t20a, t20, t22a, t22
tz = t42

Figure 7. Reset Inactive Timing

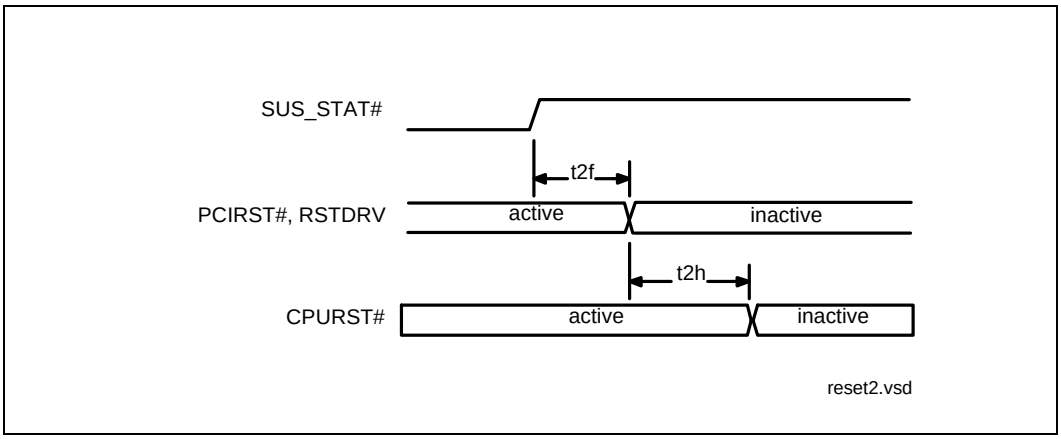


Figure 8. Reset Active Pulse Width

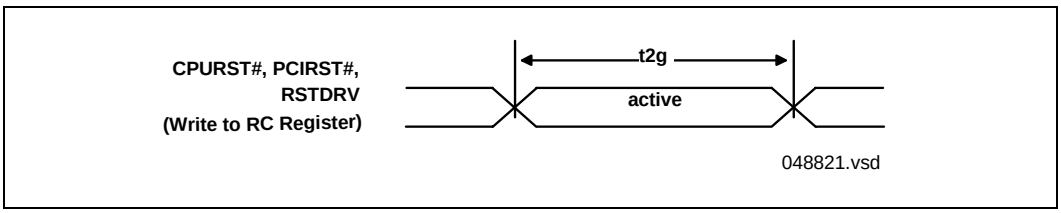


Figure 9. SMI#, EXSMI# and STPCLK# Timing

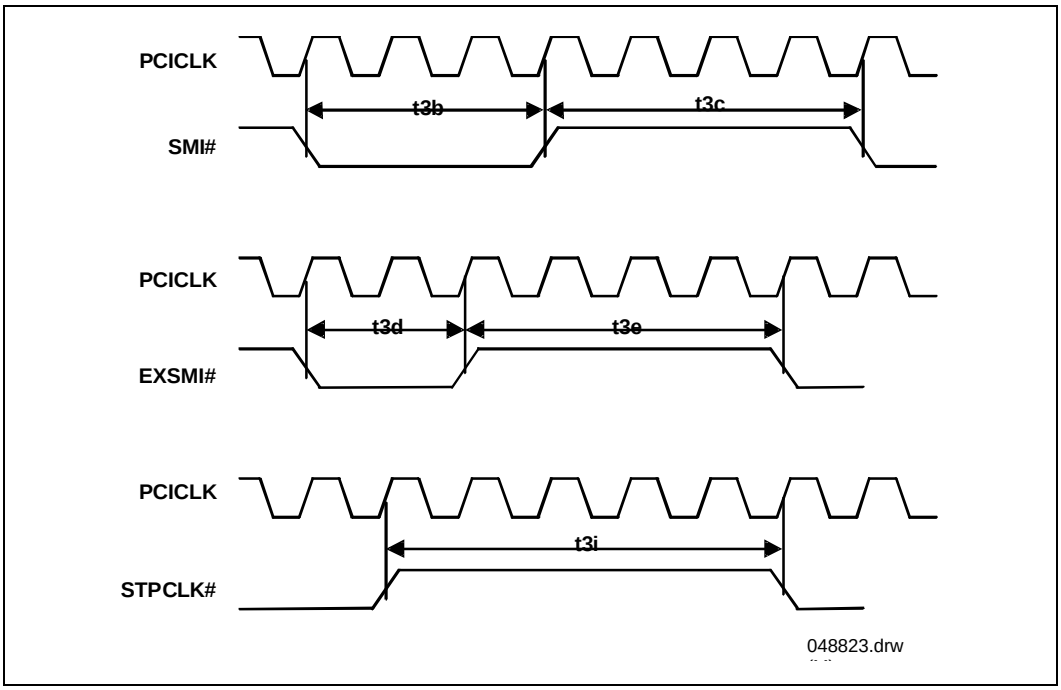


Figure 10. Input to PCICLK Setup/Hold Times

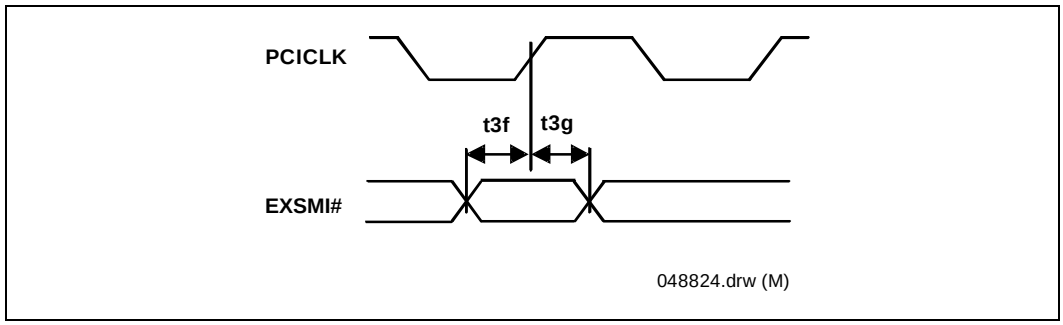


Figure 11. PCICLK to Output Valid Delay

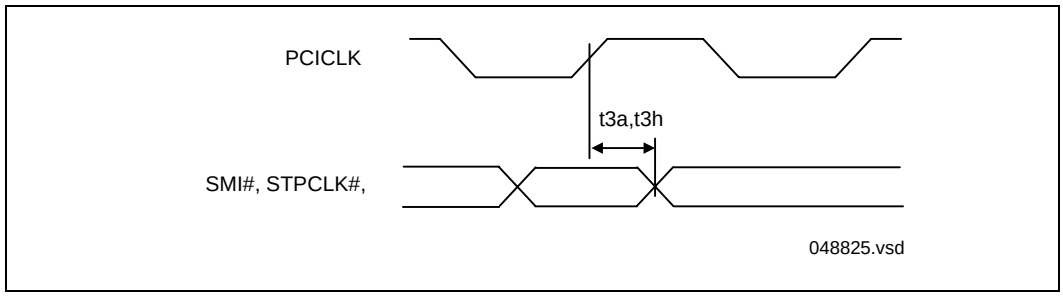


Figure 12. 8-Bit Memory Slave Timing (440MX as Master)

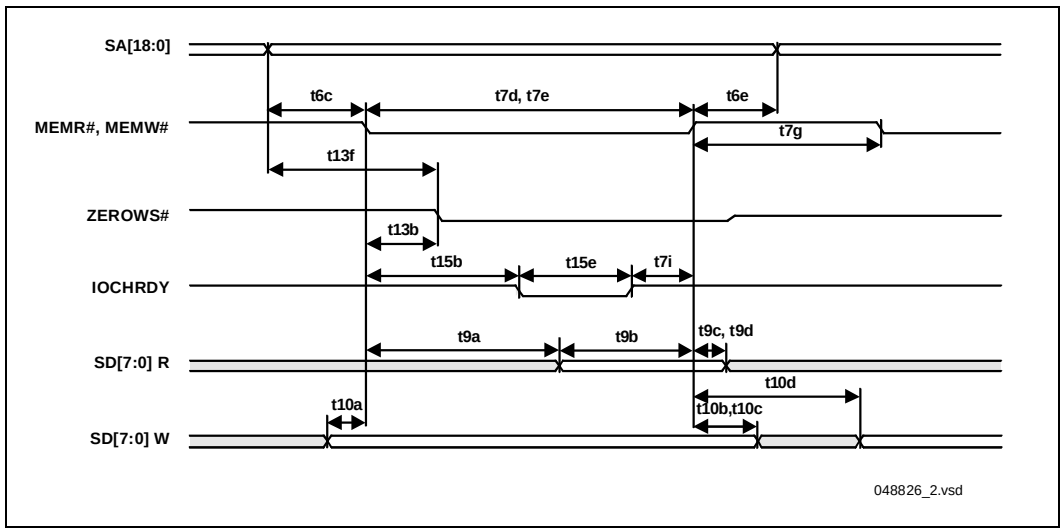


Figure 13. 8-Bit I/O Slave Timing (440MX as Master)

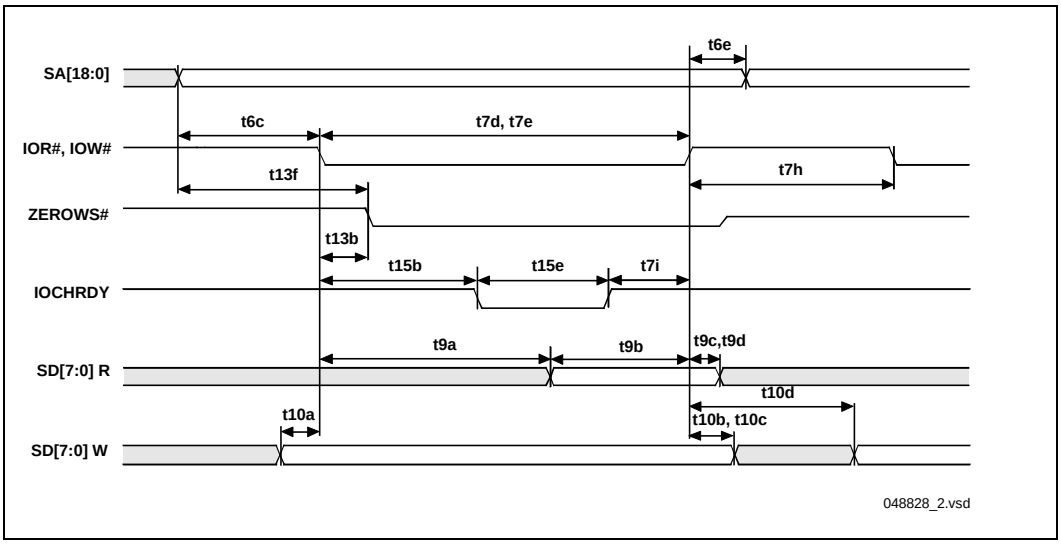


Figure 14. NMI Timing

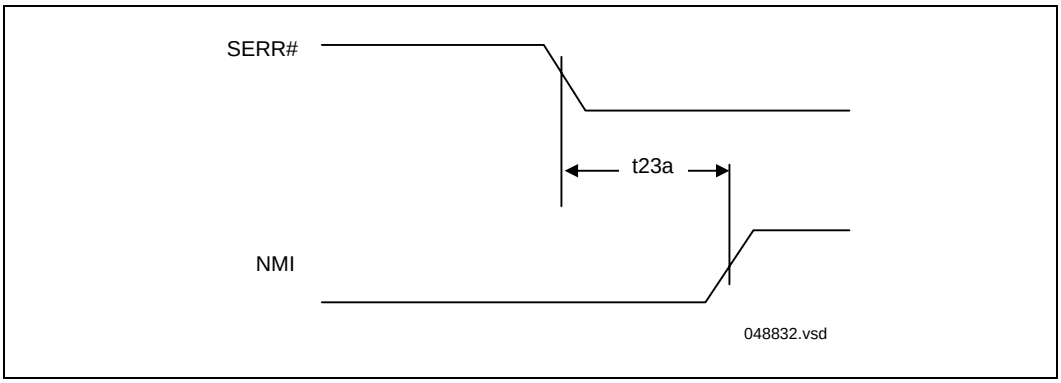


Figure 15. Interrupt Timing

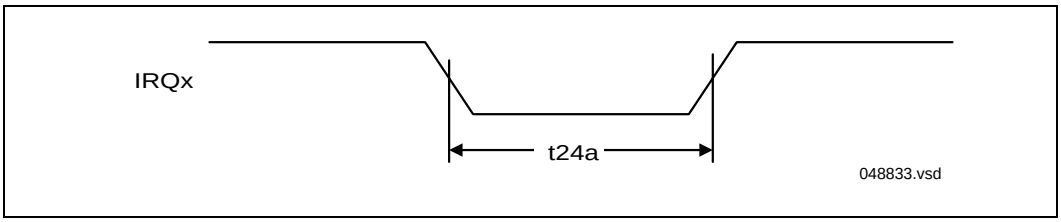


Figure 16. DMA Compatible Timing (Memory Read)

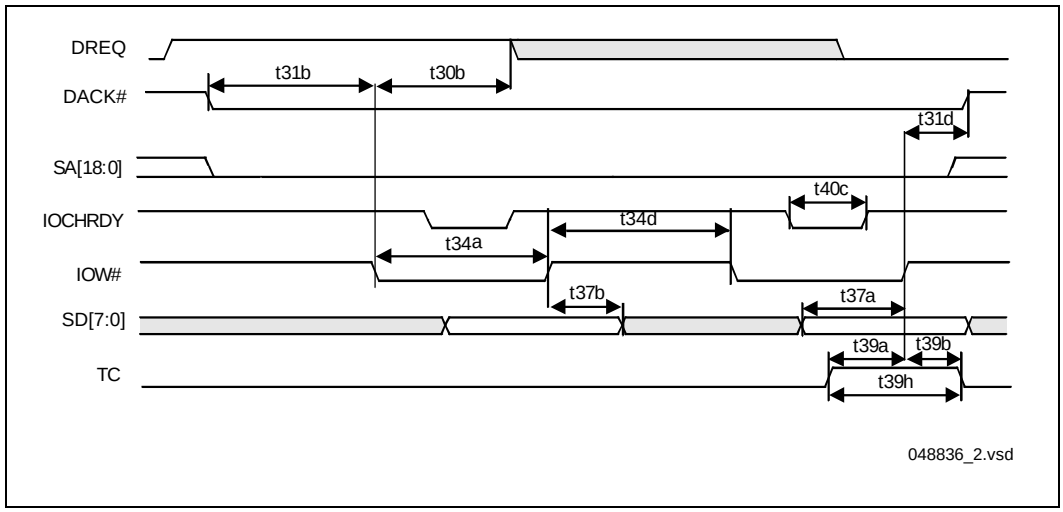


Figure 17. DMA Compatible Timing (Memory Write)

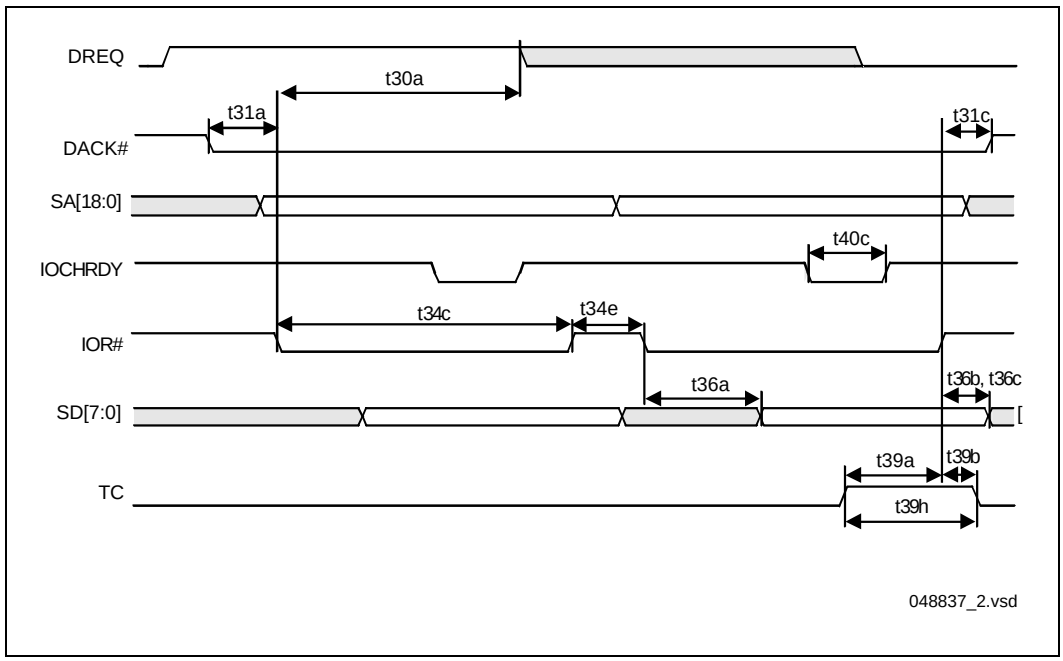


Figure 18. DMA Type F Timing

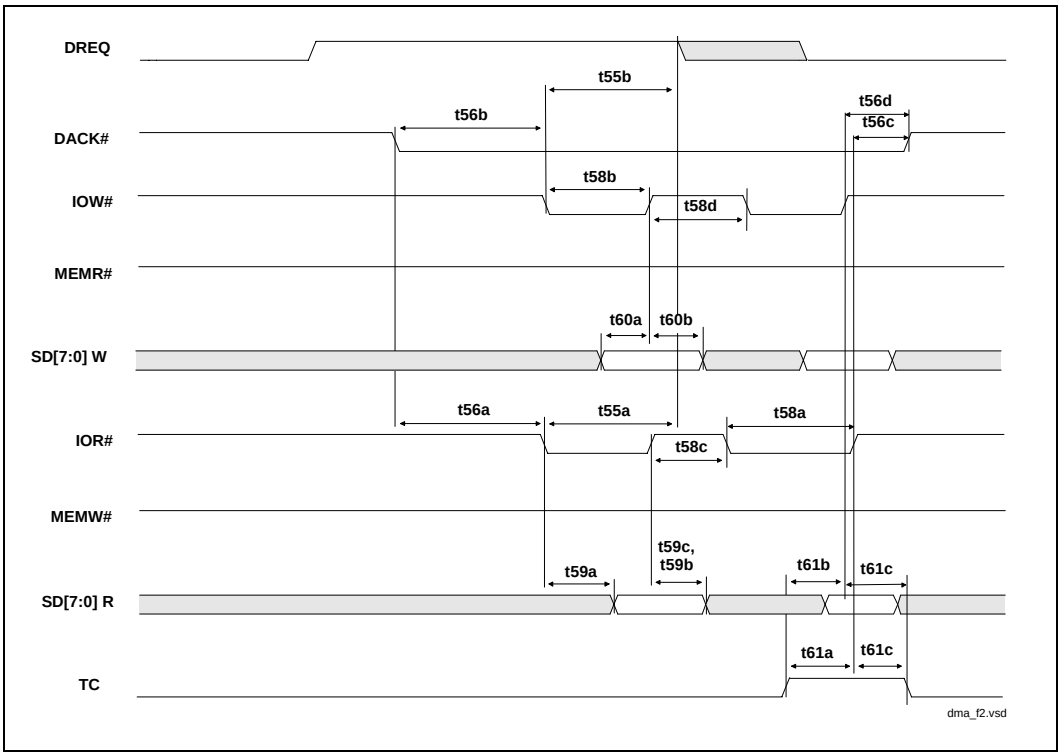


Figure 19. 440MX X-Bus Timing

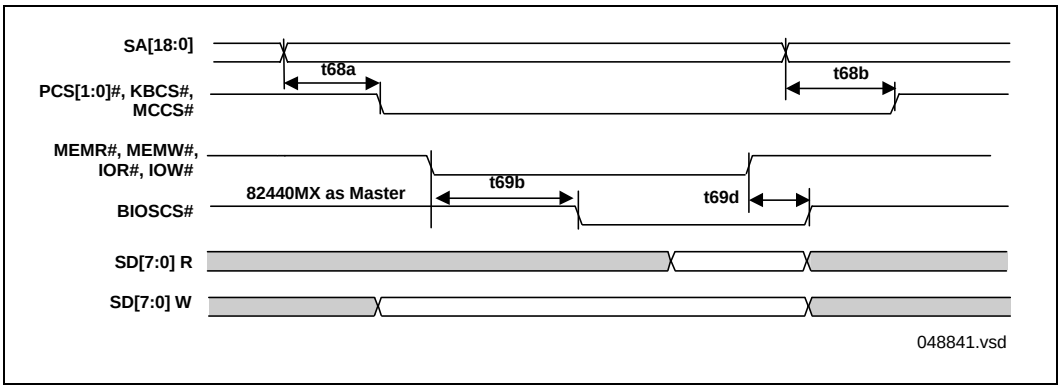


Figure 20. Coprocessor Error and Mouse Support Timing

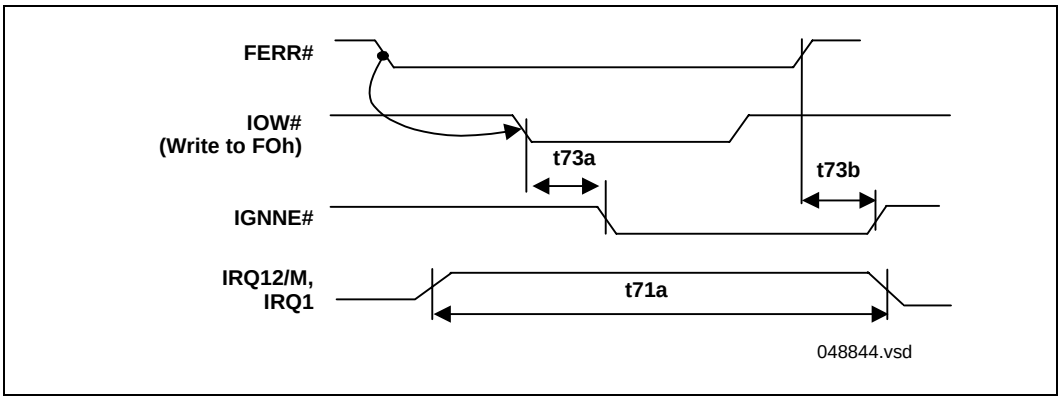
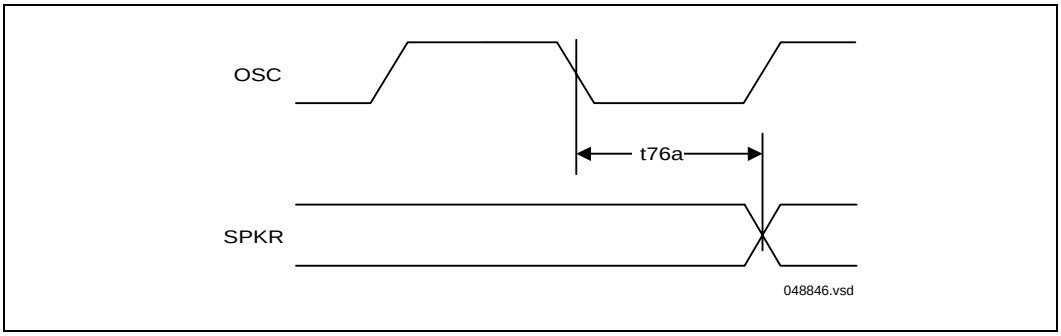


Figure 21. Speaker Timing



2.2.4 PCI Timing Diagrams

Figure 22. Propagation Delay

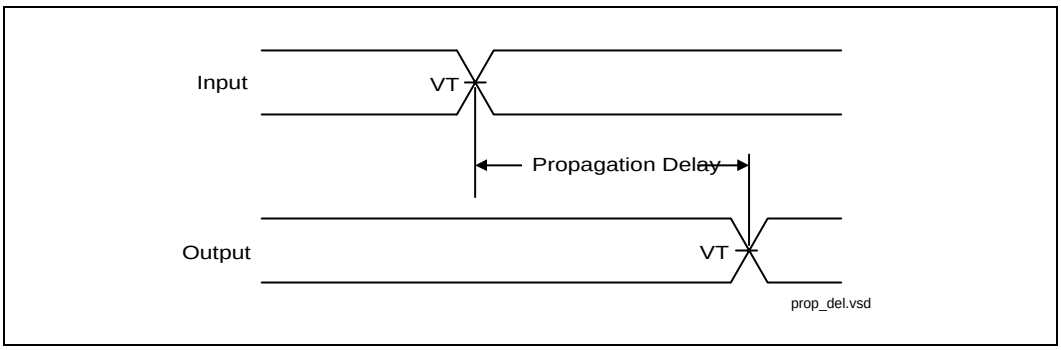
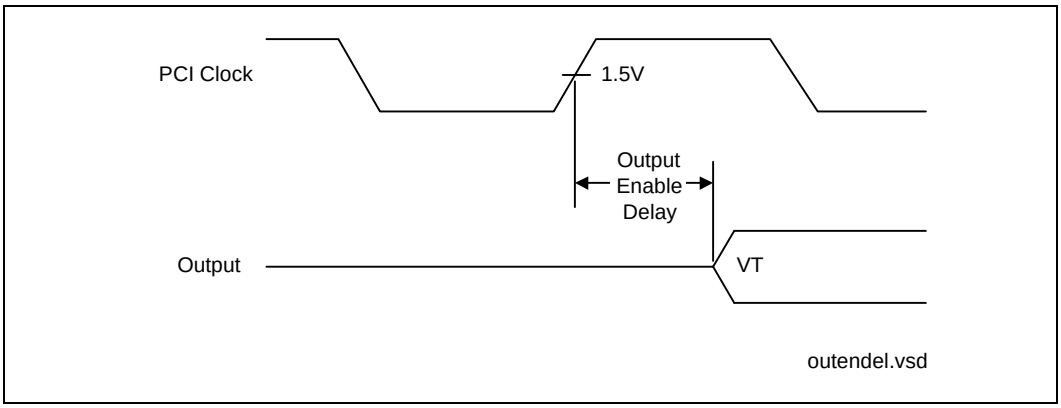


Figure 23. Output Enable Delay



2.2.5 IDE Timing Diagrams

Figure 24. IDE PIO Mode

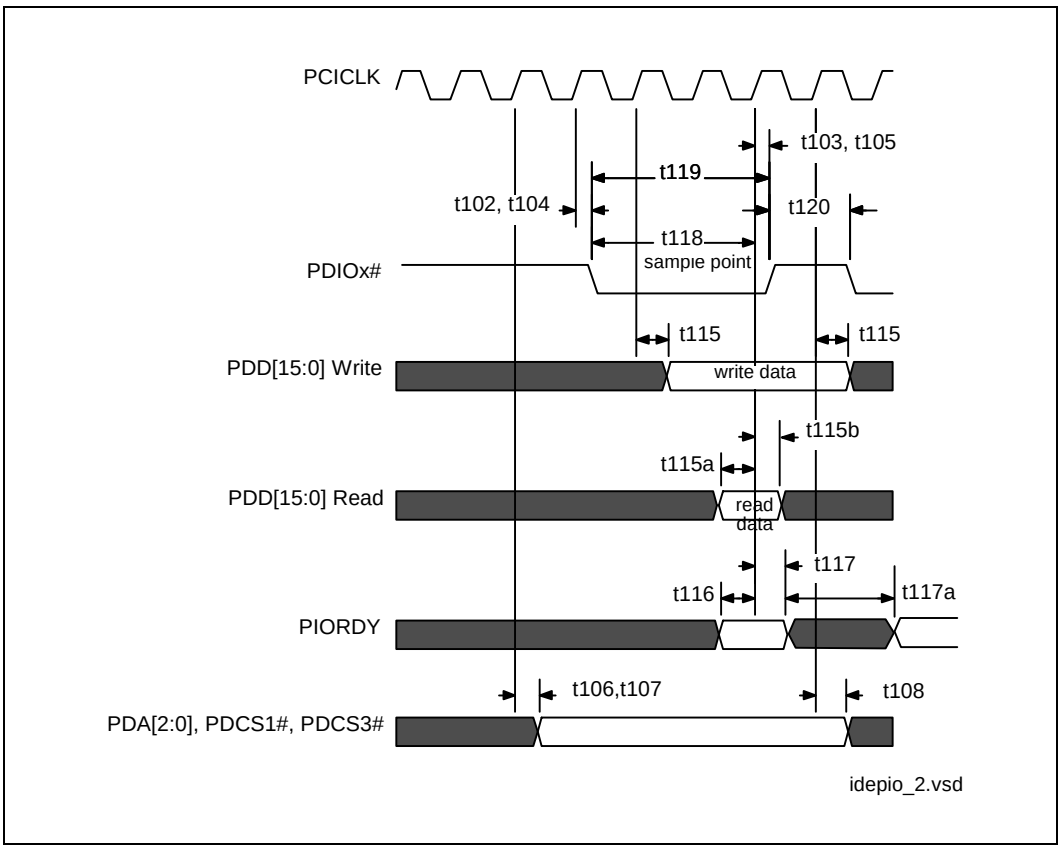
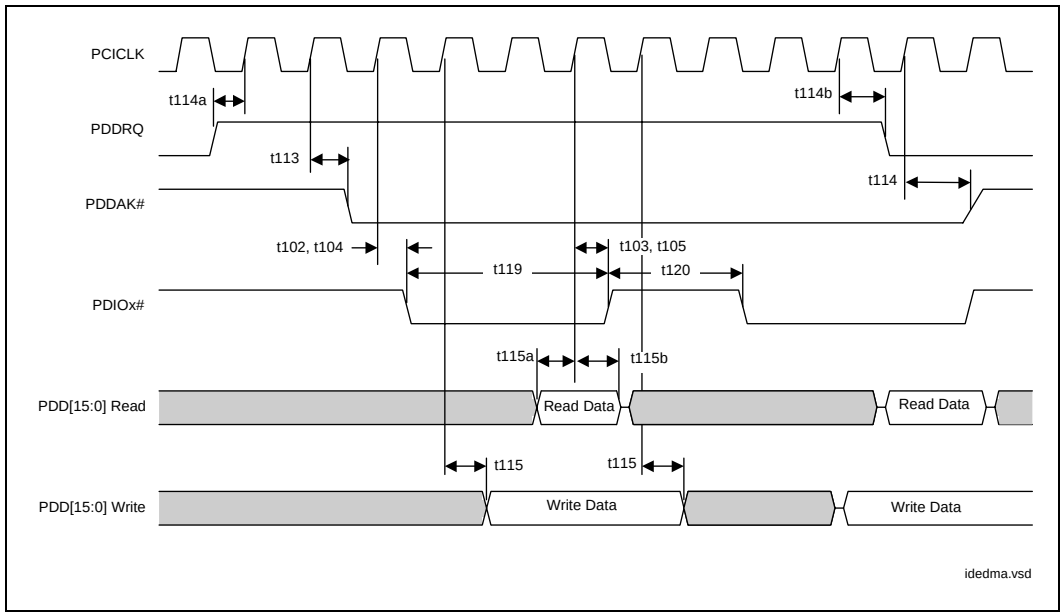
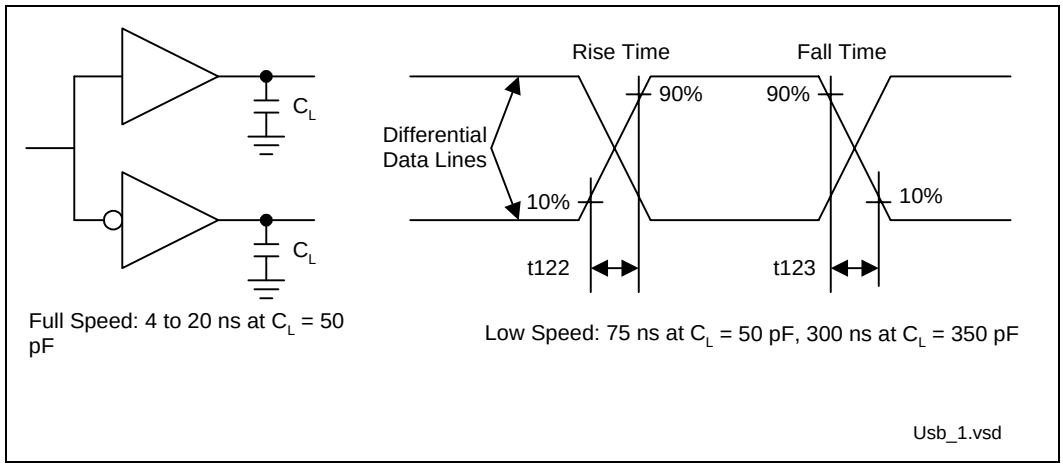


Figure 25. IDE Multiword DMA Mode



2.2.6 USB Timing Diagrams

Figure 26. Data Signal Rise and Fall Time



Full Speed: 4 to 20 ns at C_L = 50 pF

Low Speed: 75 ns at C_L = 50 pF, 300 ns at C_L = 350 pF

Figure 27. Data Jitter

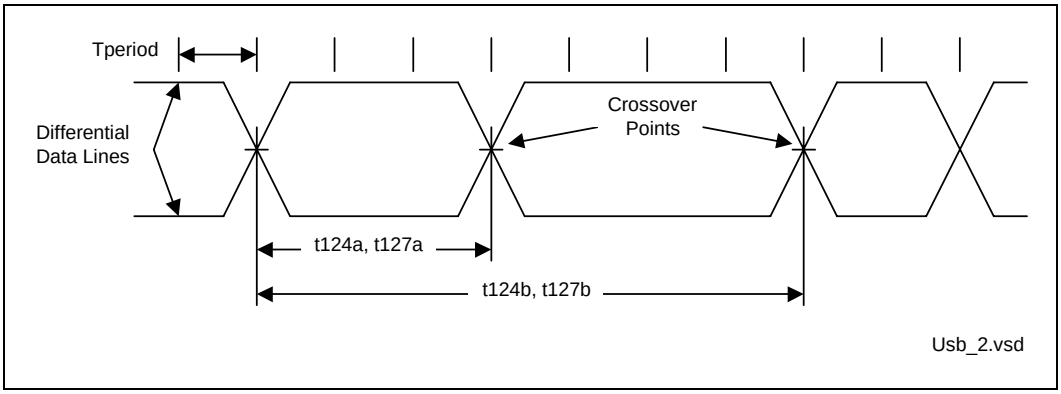
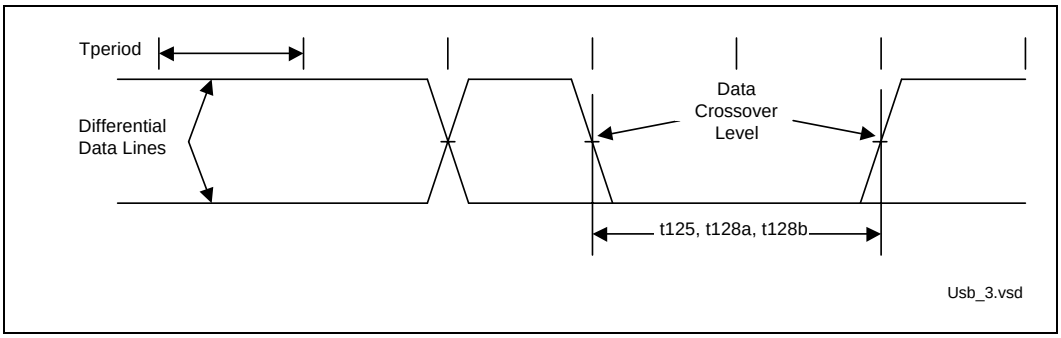


Figure 28. EOP Width Timing



2.2.7 SMBus Timing Diagrams

Figure 29. SMBus Timing

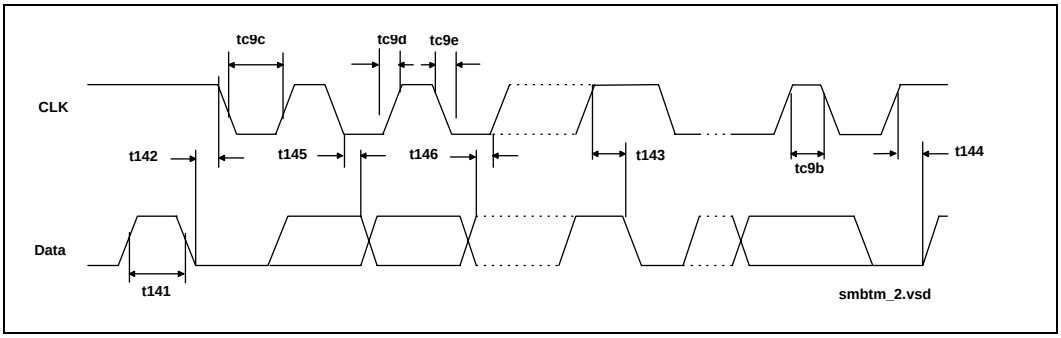
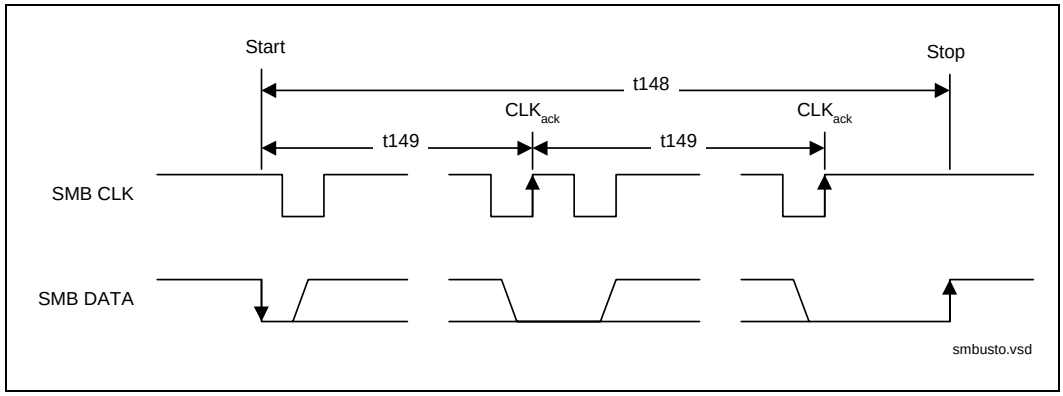


Figure 30. SMBus Timeout Timing



2.2.8 Ultra DMA/33 Timing Diagrams

Figure 31. Ultra DMA/33 Drive Initiating a DMA Burst for a Read Command

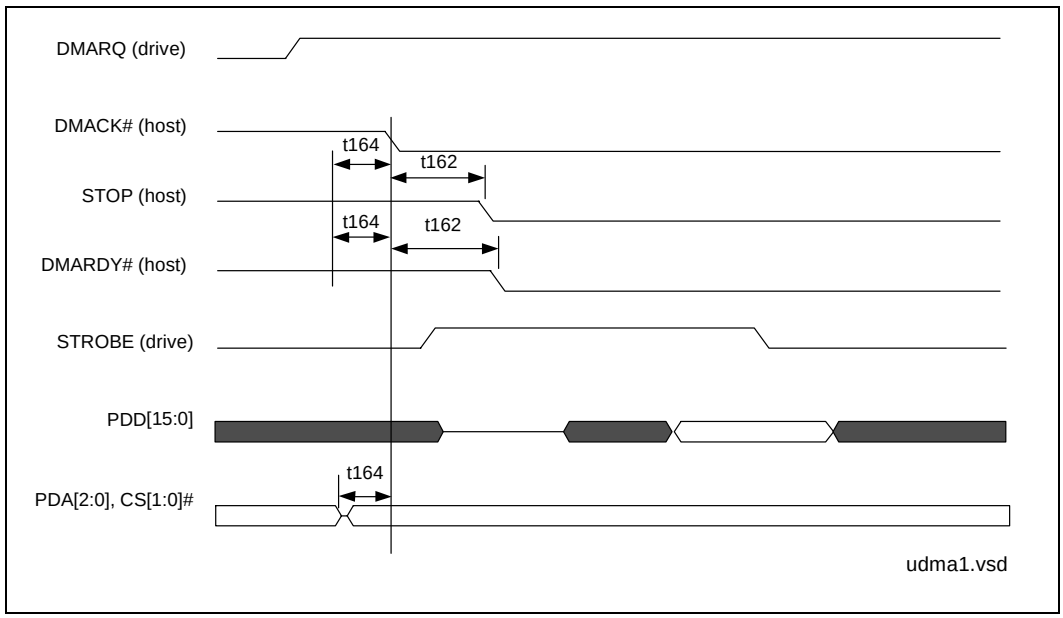


Figure 32. Ultra DMA/33 Sustained Synchronous DMA Burst

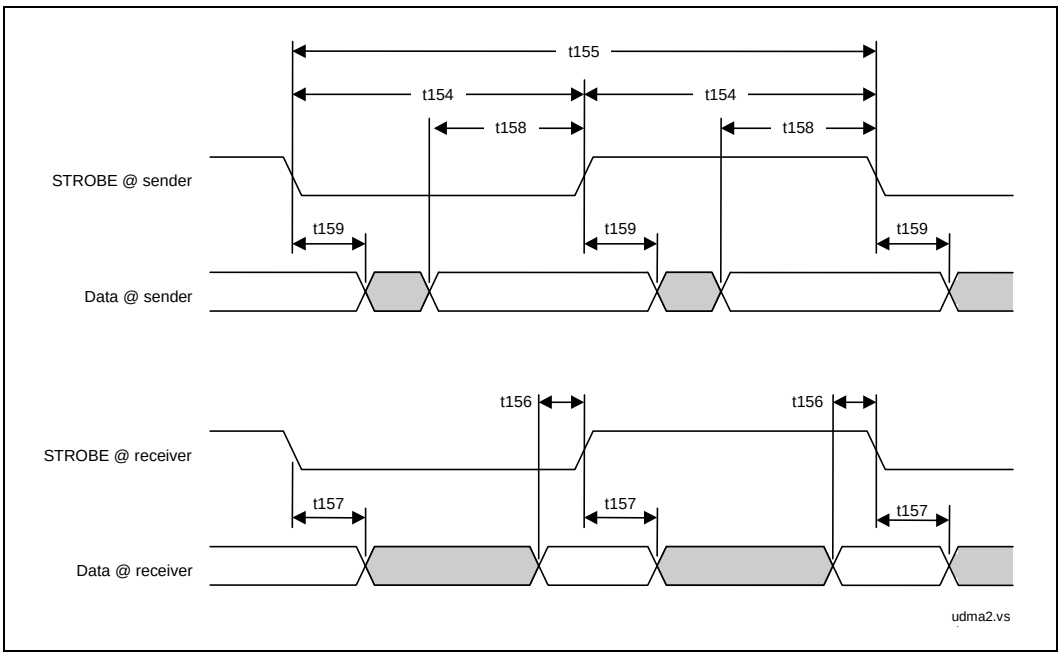


Figure 33. Ultra DMA/33 Sustained Synchronous DMA Burst

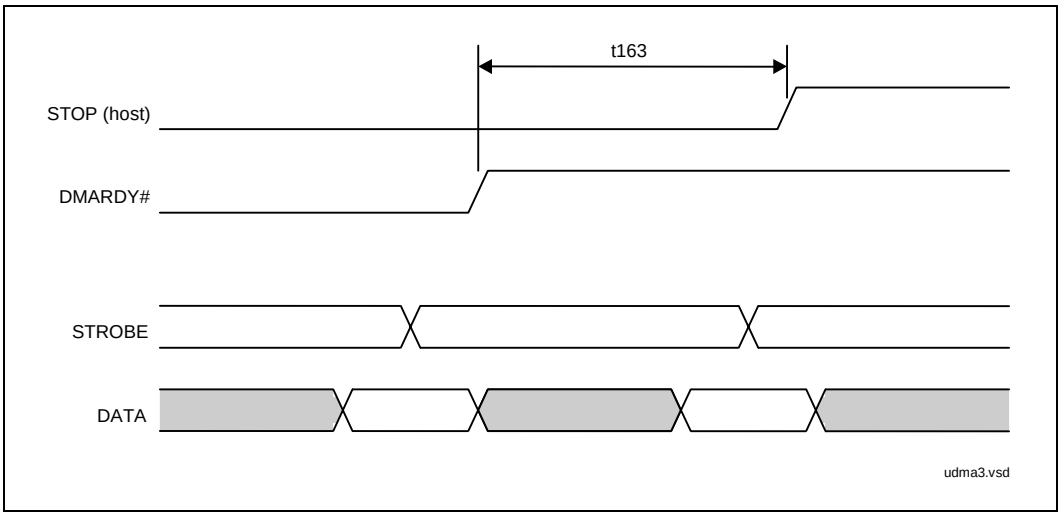
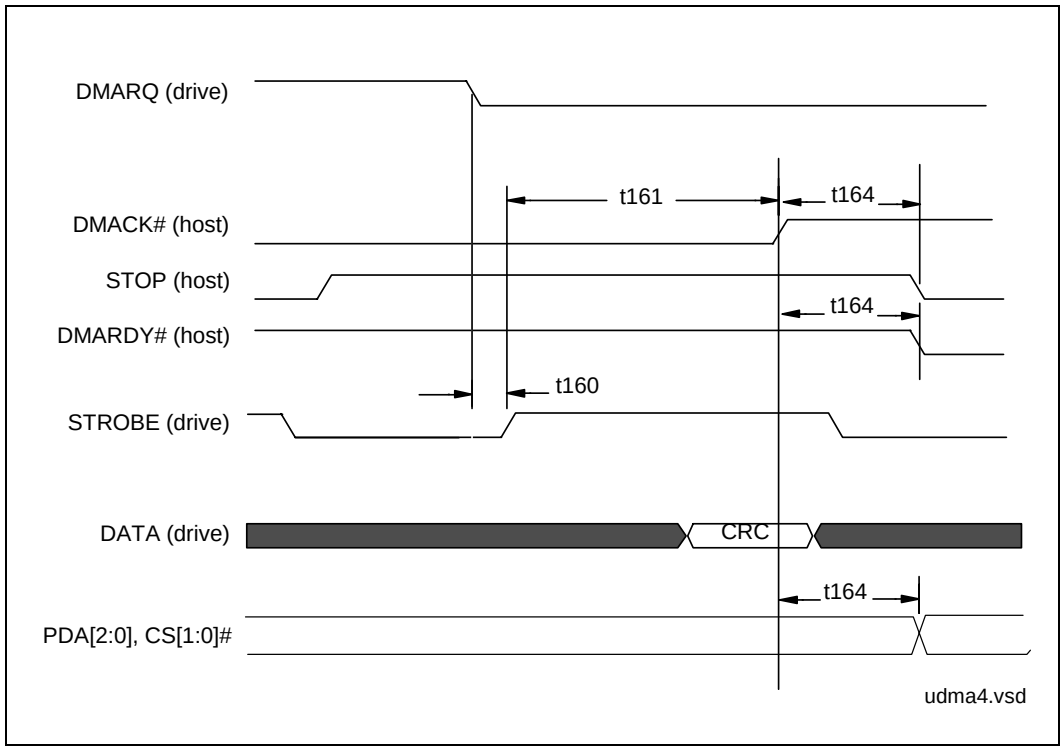


Figure 34. Ultra DMA/33 Host Terminating a DMA Burst During a Write Command



2.2.9 AC'97 Timings

Refer to Table 5 and Table 6 of this document for AC'97 timings. Refer to *AC'97 Specification 2.2*, Section 10 for timing diagrams of digital DC and AC characteristics. Available at: http://developer.intel.com/ial/scalableplatforms/audio/

3.0 440MX Power/Thermal Characteristics

3.1 Power Characteristics

Table 20. Power Characteristics

Symbol	Parameter	440MX 66 MHz TDP[3]	440MX 100 MHz TDP[3]	Unit	Notes
P_{LX}	Power Dissipation	1.7	2.10	W	1, 2

NOTE:
1. This specification is a combination of core power (I_{CC}) and power dissipated in the GTL+ outputs and I/O.
2. Not 100% tested. Specified by design characterization
3. TDP (Thermal Design Power)

3.2 Thermal Management Introduction

In a system environment, the chipset temperature is a function of both the system and component thermal characteristics. The system level thermal constraints consist of the local ambient temperature at the component, the airflow over the component and surrounding board as well as the physical constraints at, above, and surrounding the component. The component's case temperature depends on the component power dissipation, size, packaging materials (effective thermal conductivity), the type of interconnection to the substrate and motherboard, the presence of a thermal cooling solution, the thermal conductivity, the power density of the substrate, and the nearby components and motherboard.

3.2.1 Importance of Thermal Management

The objective of thermal management is to ensure that the temperature of all components in a system are maintained within functional limits. The functional temperature limit is the range within which the electrical circuits can be expected to meet specified performance requirements. Operation outside the functional limit can degrade system performance, cause logic errors or cause component and/or system damage. Temperatures exceeding the maximum operating limits may result in irreversible changes in the operating characteristics of the component.

3.2.2 Thermal Specifications

To ensure proper operation and reliability of the 440MX, the thermal solution must maintain a case temperature (T_{CASE}) at or below its specified value (Table 21). Considering the power dissipation levels and typical system ambient environments of 50° C to 70° C, if the 440MX case temperature exceeds the maximum case temperature listed in Table 21, system or component level thermal enhancements will be required to dissipate the generated heat. In general, systems should be designed to dissipate the highest possible thermal power.

Table 21. 440MX Thermal Absolute Maximum Ratings

Parameter	Maximum	Note
T_{CASE}	95 °C	T_{CASE} is defined as the maximum case temperature without any thermal enhancement to the package.

3.2.3 Case Temperature

The case temperature is a function of the local ambient temperature and the internal temperatures of the 440MX. As a local ambient temperature is not specified for the 440MX, the only restriction is that the maximum case temperature (T_{CASE}) is not exceeded. Note that increasing the heat flow through the case increases the difference in temperature between the junction and case, reducing the maximum allowable case temperature.

3.2.4 Measurements for Thermal Specifications

Proper measurements must be made to appropriately determine the thermal properties of the system. Section 3.2.5 provides guidelines to accurately measure the case temperature of the 440MX.

3.2.5 Case Temperature Measurements

To ensure functionality and reliability, the 440MX is specified for proper operation when T_{CASE} is maintained at or below the maximum case temperature listed in Table 21. The surface temperature of the case in the geometric center of the mold cap is measured. Special care is required when measuring T_{CASE} to ensure an accurate temperature measurement.

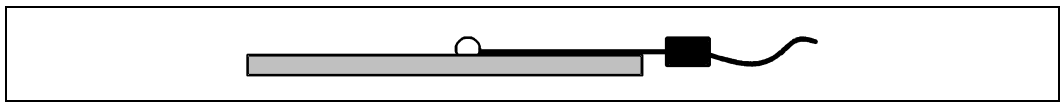
Thermocouples are often used to measure T_{CASE}. Before any temperature measurements are made, the thermocouples must be calibrated.

When a surface temperature measurement differs from the surrounding local ambient air temperature, errors could be introduced in the measurements. These measurement errors may result from having a poor thermal contact between the thermocouple junction and the surface of the package, heat loss by radiation, convection, by conduction through thermocouple leads, or by contact between the thermocouple cement and the heat-sink base for heat-sink solutions. To minimize these measurement errors, the following approach is recommended:

Attaching the thermocouple:

- Use 36 gauge or smaller diameter T type thermocouples.
- Ensure that the thermocouple has been properly calibrated.
- Attach the thermocouple bead or junction to the top surface of the package (case) in the center of the mold-cap using high thermal conductivity cements. An alternative for tape attach users is to use the tape itself to mount the thermocouple. **It is critical that the thermocouple be closely connected across the entire moldcap.**
- The thermocouple should be attached at a 0° angle if there is no interference with the thermocouple attach location or leads (see Figure 35). This is the preferred method and is recommended for use with both unenhanced packages as well as packages employing thermal enhancements.

Figure 35. Technique for Measuring T_{CASE} with 0° Angle Attachment



- If the thermocouple cannot be attached as shown in Figure 35, the thermocouple may be attached at a 90° angle (see Figure 36).
- The hole size through the heat sink base to route the thermocouple wires out should be smaller than 0.150” in diameter.
- Make sure there is no contact between the thermocouple cement and heat sink base. This contact will affect the thermocouple reading.

Figure 36. Technique for Measuring T_{CASE} with 90° Angle Attachment