November 1998

National Semiconductor

54AC163 • 54ACT163
Synchronous Presettable Binary Counter

General Description

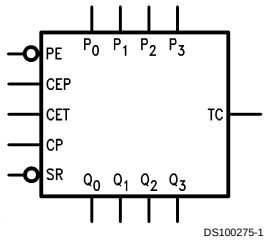
The 'AC/'ACT163 are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'AC/'ACT163 has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

- Synchronous counting and loading
- High-speed synchronous expansion
- Typical count rate of 125 MHz
- Outputs source/sink 24 mA
- 'ACT163 has TTL-compatible inputs
- Standard Microcircuit Drawing (SMD)
  - — 'AC163: 5962-89582
  - — 'ACT163: 5962-91723

Features

- I_{CC} reduced by 50%

Logic Symbols



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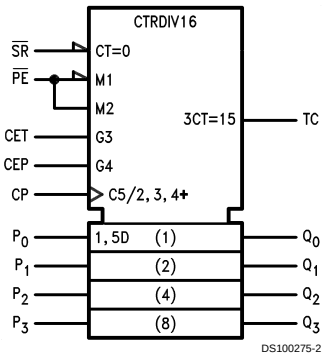
IEEE/IEC



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Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input
$\overline{SR}$	Synchronous Reset Input
P_0–P_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input
Q_0–Q_3	Flip-Flop Outputs
TC	Terminal Count Output

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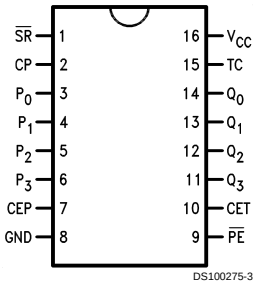
Connection Diagrams

Pin Assignment for DIP and Flatpak



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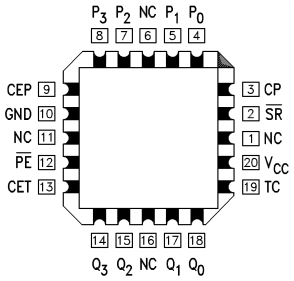
Pin Assignment for LCC



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Functional Description

The 'AC/'ACT163 counts in modulo-16 binary sequence. From state 15 (HHHH) it increments to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: synchronous reset, parallel load, count-up and hold. Four control inputs — Synchronous Reset ($\overline{SR}$), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{SR}$ HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 'AC/'ACT163 uses D-type edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways.

Figure 1 shows the connections for simple ripple carry, in which the clock period must be longer than the CP to $\overline{TC}$ delay of the first stage, plus the cumulative $\overline{CET}$ to $\overline{TC}$ delays of the intermediate stages, plus the $\overline{CET}$ to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry lookahead connections shown in *Figure 2* are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the Up mode, or min to max in the Down mode, to start its final cycle. Since this final cycle takes 16 clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to $\overline{TC}$ delay of the first stage plus the $\overline{CEP}$ to CP setup time of the last stage. The $\overline{TC}$ output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers or counters.

Logic Equations: Count Enable = CEP • CET • $\overline{PE}$

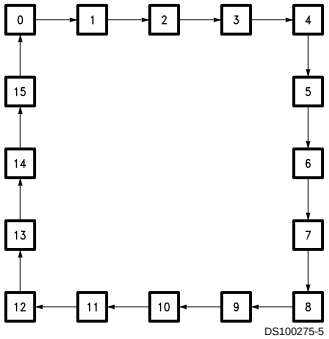
$TC = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet CET$

Mode Select Table

$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (↗)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagram



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State Diagram (Continued)

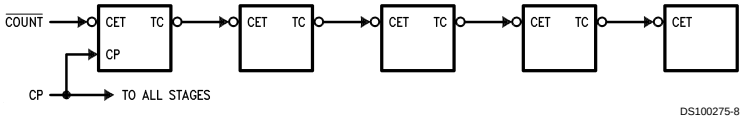

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FIGURE 1.

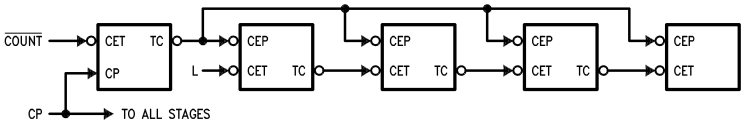

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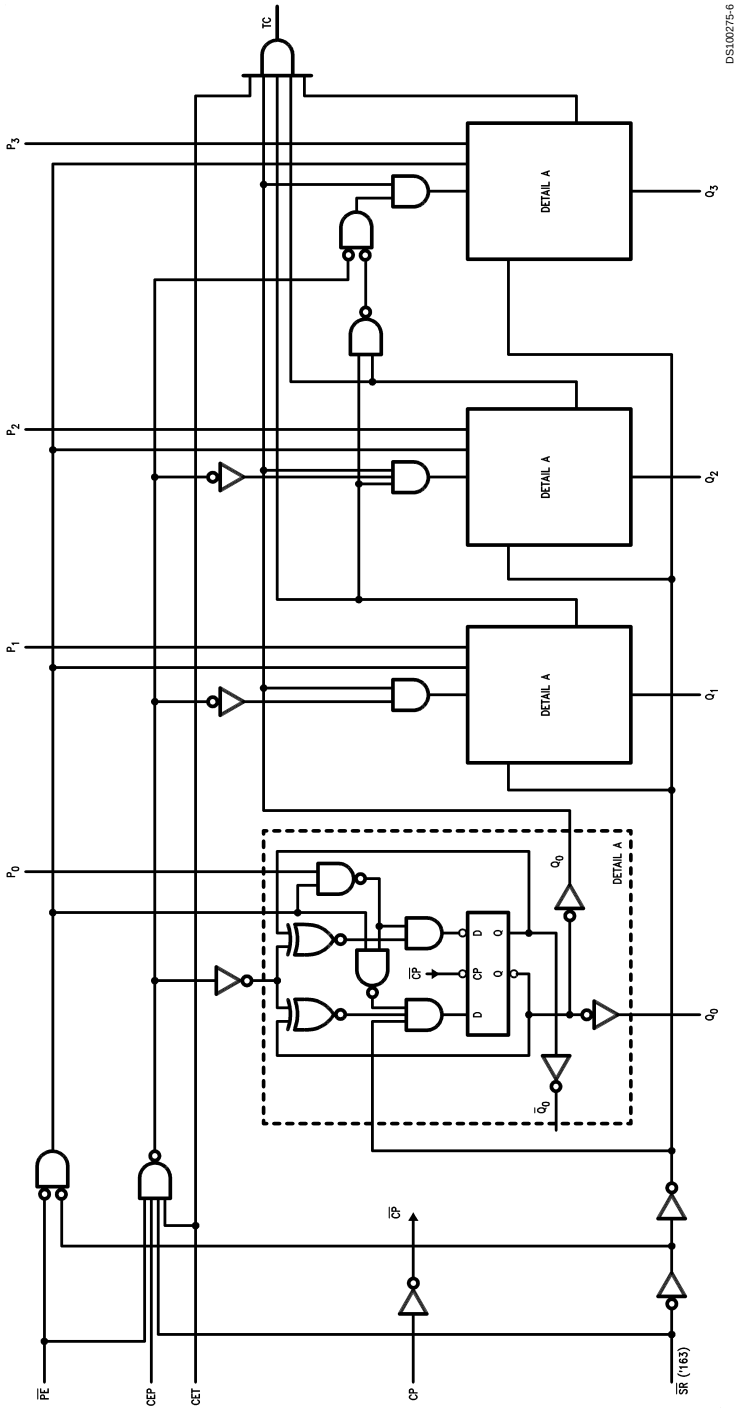
FIGURE 2.

Block Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65˚C to +150˚C
Junction Temperature (T_J)	
CDIP	175˚C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54AC/ACT	−55˚C to +125˚C
Minimum Input Edge Rate (ΔV/Δt)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	54AC T_A = −55˚C to +125˚C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	3.0	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	3.15		
		5.5	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	1.35		
		5.5	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.9	V	I_{OUT} = −50 µA
		4.5	4.4		
		5.5	5.4		
					(Note 2) V_{IN} = V_{IL} or V_{IH}
		3.0	2.4	V	I_{OH} = −12 mA
		4.5	3.7		I_{OH} = −24 mA
		5.5	4.7		I_{OH} = −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.1	V	I_{OUT} = 50 µA
		4.5	0.1		
		5.5	0.1		
					(Note 2) V_{IN} = V_{IL} or V_{IH}
		3.0	0.50	V	I_{OL} = 12 mA
		4.5	0.50		I_{OL} = 24 mA
		5.5	0.50		I_{OL} = 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	V_I = V_{CC}, GND
I_{OLD}	Minimum Dynamic Output Current (Note 3)	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V Min

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	54AC T_A = −55°C to +125°C Guaranteed Limits	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	5.5	160	µA	$V_{IN} = V_{CC}$ or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	54ACT T_A = −55°C to +125°C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage (Note 7)	4.5	3.0	V	V_{OUT} = 0.1V
		5.5	3.0		or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5	0.8	V	V_{OUT} = 0.1V
		5.5	0.8		or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5	4.4	V	I_{OUT} = −50 µA
		5.5	5.4		
					(Note 5) $V_{IN} = V_{IL}$ or 3.0V
		4.5	3.70	V	I_{OH} = −24 mA
		5.5	4.70		I_{OH} = −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.1	V	I_{OUT} = 50 µA
		5.5	0.1		
					(Note 5) $V_{IN} = V_{IL}$ or V_{IH}
		4.5	0.50	V	I_{OL} = 24 mA
		5.5	0.50		I_{OL} = 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	1.6	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	Minimum Dynamic Output Current (Note 6)	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	80.0	µA	$V_{IN} = V_{CC}$ or GND

Note 5: All outputs loaded; thresholds on input associated with output under test.

Note 6: Maximum test duration 2.0 ms, one output loaded at a time.

Note 7: For dynamic operation, a V_{IH} level between 2.0 and 3.0V may be recognized by this device as a high logic level input. For static operation, a $V_{IH} \geq 2.0V$ will be recognized by this device as a high logic level input. Users are cautioned to verify that this will not affect their system.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 8)	54AC $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF		Units
			Min	Max	
f_{max}	Maximum Clock	3.3	55		MHz
	Frequency	5.0	90		
t_{PLH}	Propagation Delay, CP to Q_n	3.3	1.0	13.5	ns
	($\overline{PE}$ Input HIGH or LOW)	5.0	1.5	9.5	
t_{PHL}	Propagation Delay, CP to Q_n	3.3	1.0	12.5	ns
	($\overline{PE}$ Input HIGH or LOW)	5.0	1.5	9.5	
t_{PLH}	Propagation Delay	3.3	1.0	16.5	ns
	CP to TC	5.0	1.5	11.0	
t_{PHL}	Propagation Delay	3.3	1.0	15.0	ns
	CP to TC	5.0	1.5	11.0	
t_{PLH}	Propagation Delay	3.3	1.0	11.0	ns
	CET to TC	5.0	1.5	7.5	
t_{PHL}	Propagation Delay	3.3	1.0	12.0	ns
	CET to TC	5.0	1.5	9.0	

Note 8: Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC} (V) (Note 9)	54AC $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF	Units
			Guaranteed Minimum	
t_s	Setup Time, HIGH or LOW	3.3	17.0	ns
	P_n to CP	5.0	11.0	
t_h	Hold Time, HIGH or LOW	3.3	−0.5	ns
	P_n to CP	5.0	0	
t_s	Setup Time, HIGH or LOW	3.3	17.0	ns
	$\overline{SR}$ to CP	5.0	12.0	
t_h	Hold Time, HIGH or LOW	3.3	−0.5	ns
	$\overline{SR}$ to CP	5.0	0	
t_s	Setup Time, HIGH or LOW	3.3	16.0	ns
	$\overline{PE}$ to CP	5.0	9.5	
t_h	Hold Time, HIGH or LOW	3.3	−0.5	ns
	$\overline{PE}$ to CP	5.0	0	
t_s	Setup Time, HIGH or LOW	3.3	8.0	ns
	CEP or CET to CP	5.0	5.5	
t_h	Hold Time, HIGH or LOW	3.3	0	ns
	CEP or CET to CP	5.0	0.5	
t_w	Clock Pulse Width (Load)	3.3	5.0	ns
	HIGH or LOW	5.0	5.0	
t_w	Clock Pulse Width (Count)	3.3	5.0	ns
	HIGH or LOW	5.0	5.0	

Note 9: Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 10)	54ACT $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF		Units
			Min	Max	
f_{max}	Maximum Clock Frequency	5.0	90		MHz
t_{PLH}	Propagation Delay, CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.5	10.5	ns
t_{PHL}	Propagation Delay, CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.5	10.5	ns
t_{PLH}	Propagation Delay CP to TC	5.0	1.5	12.5	ns
t_{PHL}	Propagation Delay CP to TC	5.0	1.5	13.0	ns
t_{PLH}	Propagation Delay CET to TC	5.0	1.5	9.5	ns
t_{PHL}	Propagation Delay CET to TC	5.0	1.5	9.5	ns

Note 10: Voltage Range 5.0 is 5.0V ±0.5V

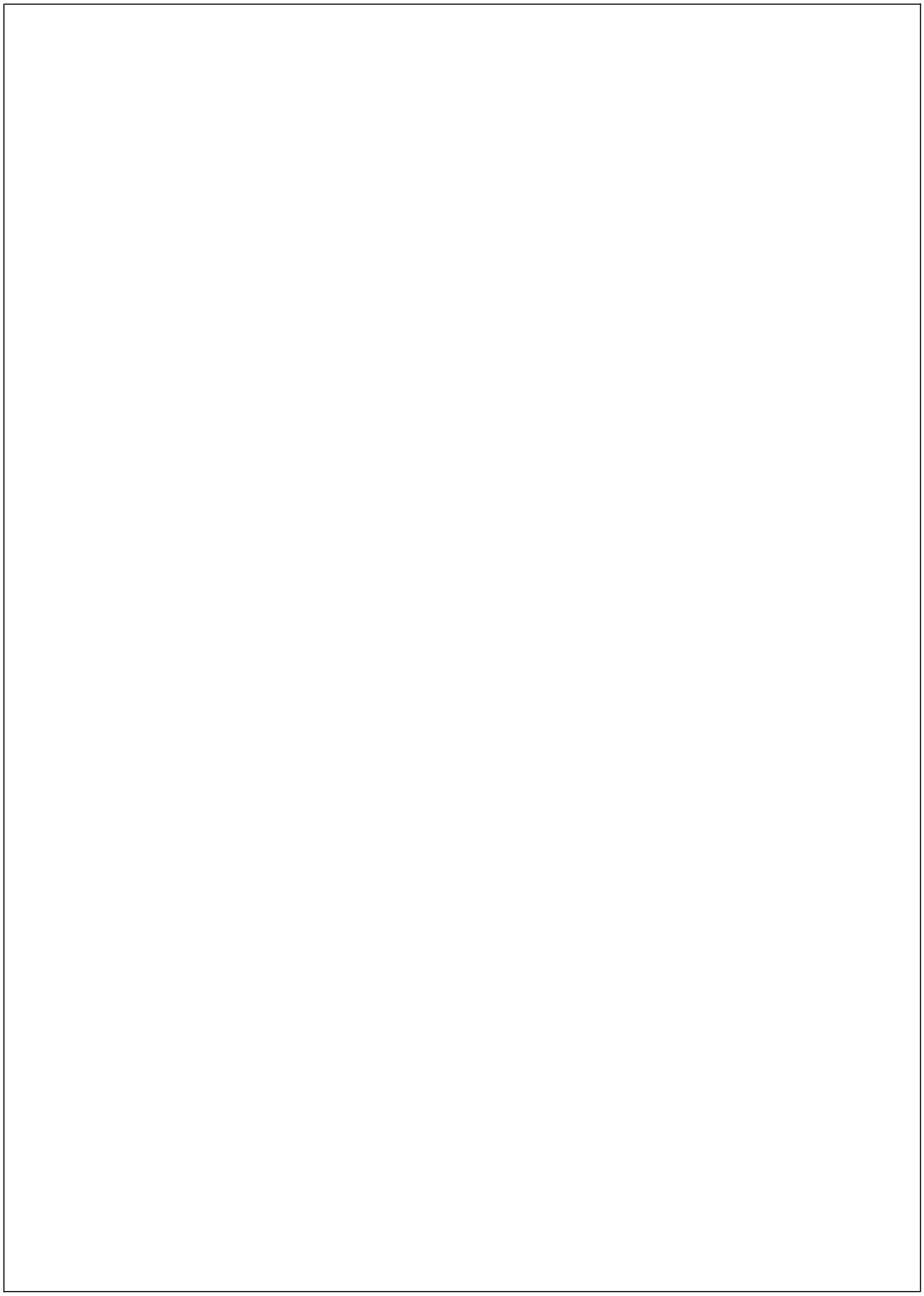
AC Operating Requirements

Symbol	Parameter	V_{CC} (V) (Note 11)	54ACT $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF	Units
			Guaranteed Minimum	
t_s	Setup Time, HIGH or LOW P_n to CP	5.0	13.5	ns
t_h	Hold Time, HIGH or LOW P_n to CP	5.0	0.5	ns
t_s	Setup Time, HIGH or LOW $\overline{SR}$ to CP	5.0	13.5	ns
t_h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	5.0	0.0	ns
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	5.0	11.5	ns
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	5.0	0.0	ns
t_s	Setup Time, HIGH or LOW CEP or CET to CP	5.0	7.0	ns
t_h	Hold Time, HIGH or LOW CEP or CET to CP	5.0	0.5	ns
t_w	Clock Pulse Width (Load) HIGH or LOW	5.0	5.0	ns
t_w	Clock Pulse Width (Count) HIGH or LOW	5.0	5.0	ns

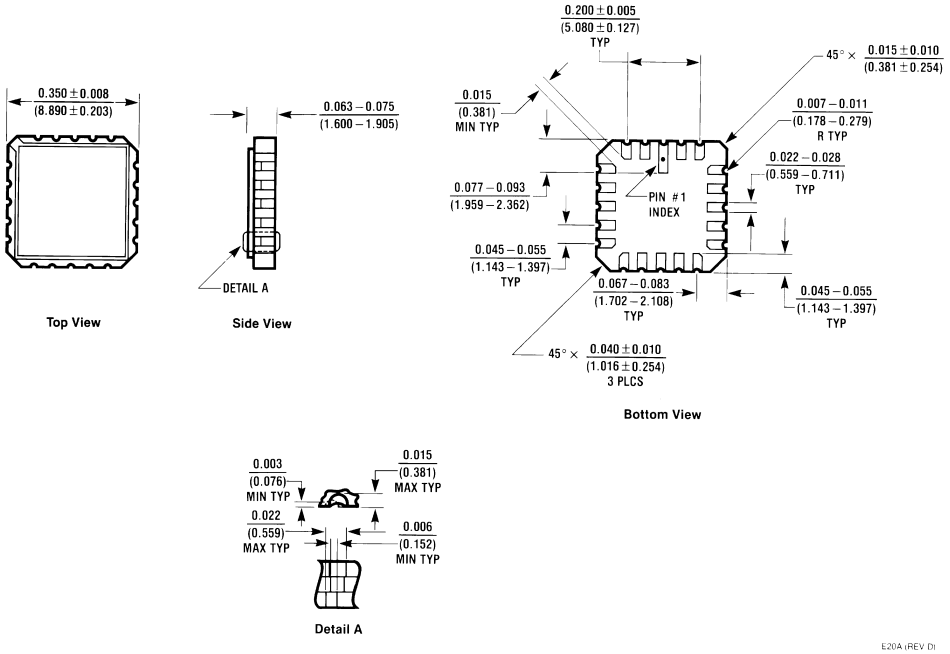
Note 11: Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

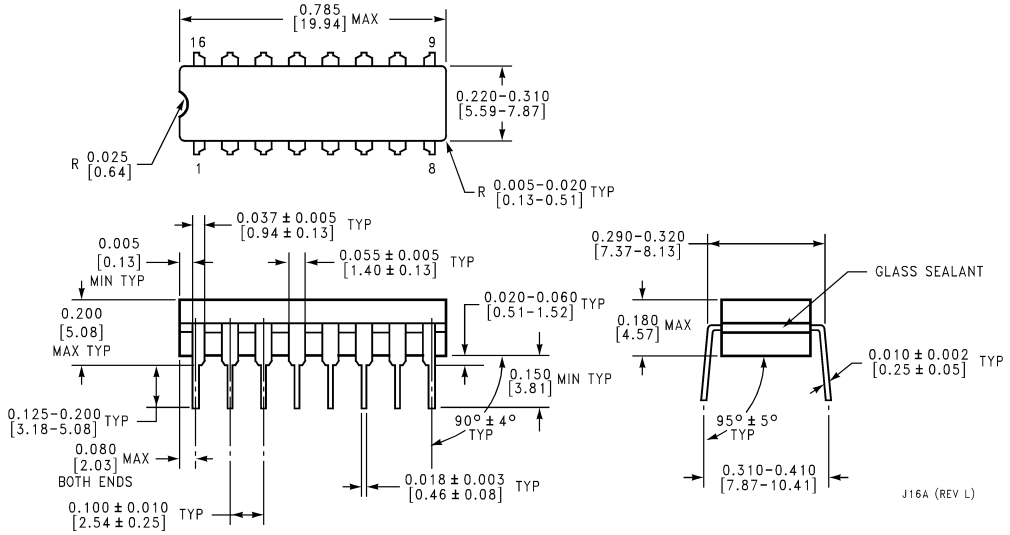
Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	45.0	pF	V_{CC} = 5.0V



Physical Dimensions inches (millimeters) unless otherwise noted

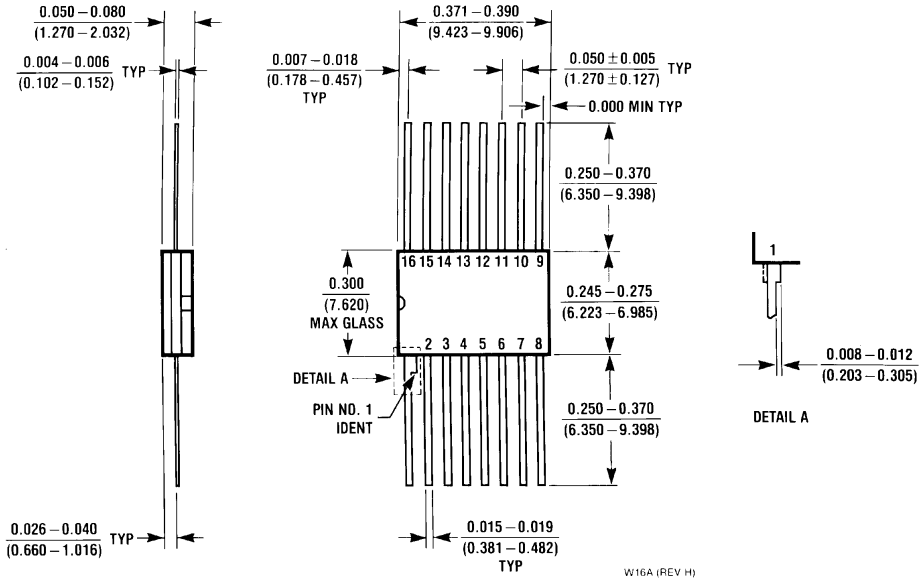


20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A



16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flatpak (F)
NS Package Number W16A

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