54AC169 • 54ACT169 4-Stage Synchronous Bidirectional Counter

Check for Samples: 54AC169, 54ACT169

FEATURES

- **I_{CC} reduced by 50%**
- **Synchronous counting and loading**
- **Built-In lookahead carry capability**
- **Presettable for programmable operation**
- **Outputs source/sink 24 mA**
- **'ACT has TTL-compatible inputs**
- **Standard Microcircuit Drawing (SMD)**
  - **5962-91603**

DESCRIPTION

The 'AC/'ACT169 is fully synchronous 4-stage up/down counter. The 'AC/'ACT169 is a modulo-16 binary counter. It features a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the Clock.

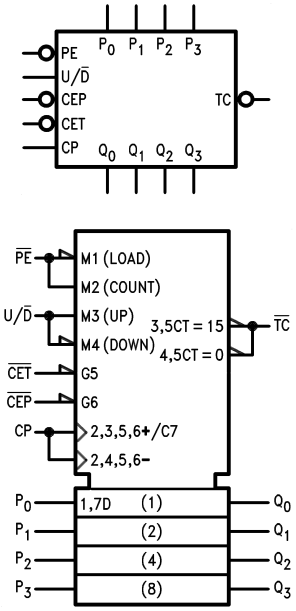


Figure 1. IEEE/IEC

Pin Names	Description
$\overline{CEP}$	Count Enable Parallel Input
$\overline{CET}$	Count Enable Trickle Input
CP	Clock Pulse Input
P_0–P_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input
U/$\overline{D}$	Up-Down Count Control Input
Q_0–Q_3	Flip-Flop Outputs
$\overline{TC}$	Terminal Count Output

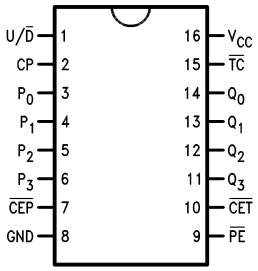


Figure 2. Pin Assignment for DIP and Flatpak

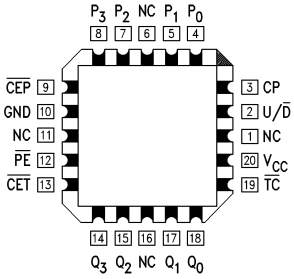
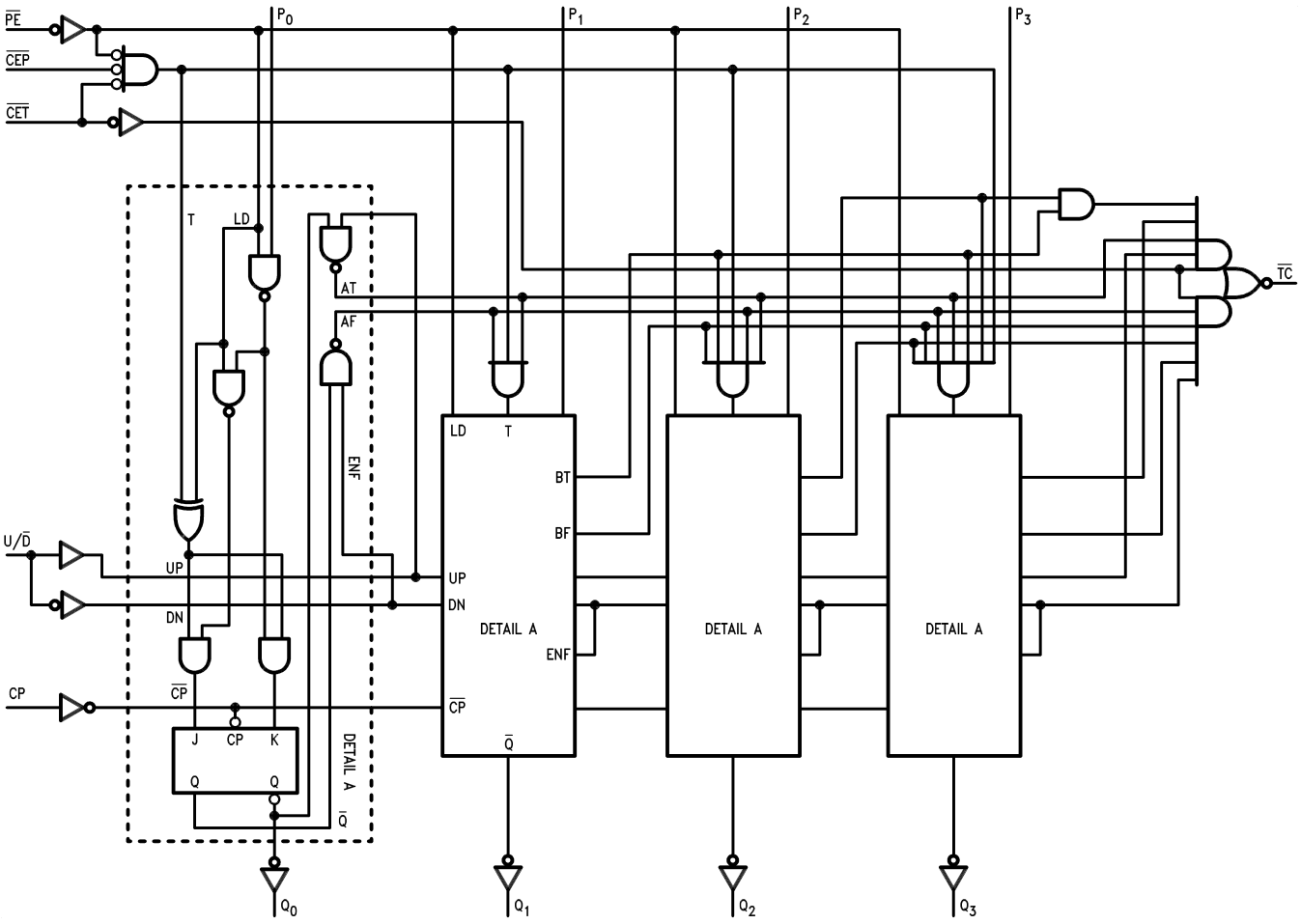


Figure 3. Pin Assignment for LCC

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

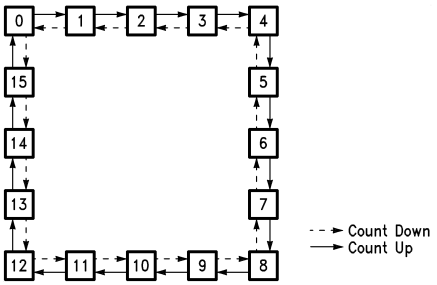
The 'AC/'ACT169 uses edge-triggered J-K-type flip-flops and have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is LOW, the data on the P_0–P_3 inputs enters the flip-flops on the next rising edge of the Clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be LOW and $\overline{PE}$ must be HIGH; the U/$\overline{D}$ input then determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW, provided that $\overline{CET}$ is LOW, when a counter reaches zero in the Count Down mode or reaches 15 in the Count Up mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. If an illegal state occurs, the 'AC169 will return to the legitimate sequence within two counts. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended (see logic equations below).

1. Count Enable = $\overline{CEP}$ •$\overline{CET}$ • $\overline{PE}$
2. Up: $\overline{TC}$ = Q_0•Q_1•$Q_2$$Q_3$•(Up)•$\overline{CET}$
3. Down: $\overline{TC}$ = $\overline{Q}_0$• $\overline{Q}_1$•$\overline{Q}_2$•$\overline{Q}_3$ •(Down)•$\overline{CET}$

Table 1. Mode Select Table

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load (P_n to Q_n)
H	L	L	H	Count Up (Increment)
H	L	L	L	Count Down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

State Diagrams



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source	
or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C

(1) Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended OperatingConditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	

Recommended OperatingConditions (continued)

54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

			54AC		
Symbol	**Parameter**	**V_{CC}**	**T_A =**	**Units**	**Conditions**
		(V)	**−55°C to +125°C**		
			Guaranteed Limits		
V_{IH}	Minimum High Level	3.0	2.1		V_{OUT} = 0.1V
	Input Voltage	4.5	3.15	V	or V_{CC} − 0.1V
		5.5	3.85		
V_{IL}	Maximum Low Level	3.0	0.9		V_{OUT} = 0.1V
	Input Voltage	4.5	1.35	V	or V_{CC} − 0.1V
		5.5	1.65		
V_{OH}	Minimum High Level	3.0	2.9		I_{OUT} = −50 µA
	Output Voltage	4.5	4.4	V	
		5.5	5.4		
					(1) V_{IN} = V_{IL} or V_{IH}
		3.0	2.4		I_{OH} = −12 mA
		4.5	3.7	V	I_{OH} = −24 mA
		5.5	4.7		I_{OH} = −24 mA
V_{OL}	Maximum Low Level	3.0	0.1		I_{OUT} = 50 µA
	Output Voltage	4.5	0.1	V	
		5.5	0.1		
					(1) V_{IN} = V_{IL} or V_{IH}
		3.0	0.50		I_{OL} = 12 mA
		4.5	0.50	V	I_{OL} = 24 mA
		5.5	0.50		I_{OL} = 24 mA
I_{IN}	Maximum Input	5.5	±1.0	µA	V_I = V_{CC}, GND
	Leakage Current				
I_{OLD}	Minimum Dynamic Output Current (2)	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent	5.5	80.0	µA	V_{IN} = V_{CC}
	Supply Current				or GND

(1) All outputs loaded; thresholds on input associated with output under test.
(2) Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACT Family Devices

			54ACT		
Symbol	**Parameter**	**V_{CC}**	**T_A =**	**Units**	**Conditions**
		(V)	**−55°C to +125°C**		
			Guaranteed Limits		
V_{IH}	Minimum High Level	4.5	2.0	V	V_{OUT} = 0.1V
	Input Voltage	5.5	2.0		or V_{CC} − 0.1V
V_{IL}	Maximum Low Level	4.5	0.8	V	V_{OUT} = 0.1V
	Input Voltage	5.5	0.8		or V_{CC} − 0.1V
V_{OH}	Minimum High Level	4.5	4.4	V	I_{OUT} = −50 µA
	Output Voltage	5.5	5.4		
					(1) V_{IN} = V_{IL} or V_{IH}
		4.5	3.70	V	I_{OH} = −24 mA
		5.5	4.70		I_{OH} = −24 mA
V_{OL}	Maximum Low Level	4.5	0.1	V	I_{OUT} = 50 µA
	Output Voltage	5.5	0.1		
					(1) V_{IN} = V_{IL} or V_{IH}
		4.5	0.50	V	I_{OL} = 24 mA
		5.5	0.50		I_{OL} = 24 mA
I_{IN}	Maximum Input	5.5	±1.0	µA	V_I = V_{CC}, GND
	Leakage Current				
I_{CCT}	Maximum	5.5	1.6	mA	V_I = V_{CC} − 2.1V
	I_{CC}/Input				
I_{OLD}	Minimum Dynamic Output Current (2)	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent	5.5	80.0	µA	V_{IN} = V_{CC}
	Supply Current				or GND

(1) All outputs loaded; thresholds on input associated with output under test.
(2) Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

			54AC			
		V_{CC}	T_A = −55°C			Fig.
Symbol	Parameter	(V)	to +125°C		Units	No.
		(1)	C_L = 50 pF			
			Min	Max		
f_{max}	Maximum Clock	3.3	55		MHz	
	Frequency	5.0	75			
t_{PLH}	Propagation Delay	3.3	1.0	15.0		
	CP to Q_n	5.0	1.5	12.0	ns	
	($\overline{PE}$ HIGH or LOW)					
t_{PHL}	Propagation Delay	3.3	1.0	16.5		
	CP to Q_n	5.0	1.5	13.0	ns	
	($\overline{PE}$ HIGH or LOW)					
t_{PLH}	Propagation Delay	3.3	3.0	22.0	ns	
	CP to $\overline{TC}$	5.0	3.0	16.0		
t_{PHL}	Propagation Delay	3.3	3.0	22.0	ns	
	CP to $\overline{TC}$	5.0	3.0	16.0		
t_{PLH}	Propagation Delay	3.3	1.0	18.5	ns	
	$\overline{CET}$ to $\overline{TC}$	5.0	1.5	13.0		
t_{PHL}	Propagation Delay	3.3	1.0	16.0	ns	
	$\overline{CET}$ to $\overline{TC}$	5.0	1.5	11.0		
t_{PLH}	Propagation Delay	3.3	1.0	18.5	ns	
	U/$\overline{D}$ to $\overline{TC}$	5.0	1.5	13.0		
t_{PHL}	Propagation Delay	3.3	1.0	16.5	ns	
	U/$\overline{D}$ to $\overline{TC}$	5.0	1.5	12.0		

(1) Voltage Range 3.3 is 3.3V ±0.3VVoltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

			54AC		
		V_{CC}	T_A = −55°C		Fig.
Symbol	Parameter	(V)	to +125°C	Units	No.
		(1)	C_L = 50 pF		
			Guaranteed Minimum		
t_s	Setup Time,	3.3	7.0		
	HIGH or LOW	5.0	4.5	ns	
	P_n to CP				
t_h	Hold Time, HIGH or LOW	3.3	2.0	ns	
	P_n to CP	5.0	2.5		
t_s	Setup Time,	3.3	13.5		
	HIGH or LOW	5.0	9.0	ns	
	$\overline{CEP}$ to CP				
t_h	Hold Time, HIGH or LOW	3.3	0.5	ns	
	$\overline{CEP}$ to CP	5.0	2.5		
t_s	Setup Time,	3.3	13.5		
	HIGH or LOW	5.0	9.0	ns	
	$\overline{CET}$ to CP				
t_h	Hold Time, HIGH or LOW	3.3	0.5	ns	
	$\overline{CET}$ to CP	5.0	2.5		
t_s	Setup Time,	3.3	8.5		
	HIGH or LOW	5.0	6.5	ns	
	$\overline{PE}$ to CP				
t_h	Hold Time, HIGH or LOW	3.3	0.5	ns	
	$\overline{PE}$ to CP	5.0	2.0		
t_s	Setup Time,	3.3	13.0		
	HIGH or LOW	5.0	9.0	ns	
	U/$\overline{D}$ to CP				
t_h	Hold Time, HIGH or LOW	3.3	0.5	ns	
	U/$\overline{D}$ to $\overline{CP}$	5.0	2.0		
t_w	CP Pulse Width,	3.3	5.0	ns	
	HIGH or LOW	5.0	5.0		

(1) Voltage Range 3.3 is 3.3V ±0.3VVoltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

			54ACT			
		V_{CC}	T_A = −55°C			Fig.
Symbol	Parameter	(V)	to +125°C		Units	No.
		(1)	C_L = 50 pF			
			Min	Max		
f_{max}	Maximum Clock	5.0	75		MHz	
	Frequency					
t_{PLH}	Propagation Delay					
	CP to Q_n	5.0	1.5	12.5	ns	
	($\overline{PE}$ HIGH or LOW)					
t_{PHL}	Propagation Delay					
	CP to Q_n	5.0	1.5	12.5	ns	
	($\overline{PE}$ HIGH or LOW)					
t_{PLH}	Propagation Delay	5.0	1.5	16.5	ns	
	CP to $\overline{TC}$					
t_{PHL}	Propagation Delay	5.0	1.5	16.5	ns	
	CP to $\overline{TC}$					
t_{PLH}	Propagation Delay	5.0	1.5	13.5	ns	
	$\overline{CET}$ to $\overline{TC}$					
t_{PHL}	Propagation Delay	5.0	1.5	13.5	ns	
	$\overline{CET}$ to $\overline{TC}$					
t_{PLH}	Propagation Delay	5.0	1.5	14.5	ns	
	U/$\overline{D}$ to $\overline{TC}$					
t_{PHL}	Propagation Delay	5.0	1.5	14.5	ns	
	U/$\overline{D}$ to $\overline{TC}$					

(1) Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

			54ACT		
		V_{CC}	T_A = −55°C		Fig.
Symbol	Parameter	(V)	to +125°C	Units	No.
		(1)	C_L = 50 pF		
			Guaranteed Minimum		
t_s	Setup Time,				
	HIGH or LOW	5.0	4.5	ns	
	P_n to CP				
t_h	Hold Time, HIGH or LOW	5.0	2.5	ns	
	P_n to CP				
t_s	Setup Time,				
	HIGH or LOW	5.0	9.0	ns	
	$\overline{CEP}$ to CP				
t_h	Hold Time, HIGH or LOW	5.0	2.5	ns	
	$\overline{CEP}$ to CP				
t_s	Setup Time,				
	HIGH or LOW	5.0	9.0	ns	
	$\overline{CET}$ to CP				
t_h	Hold Time, HIGH or LOW	5.0	2.5	ns	
	$\overline{CET}$ to CP				
t_s	Setup Time,				
	HIGH or LOW	5.0	6.5	ns	
	$\overline{PE}$ to CP				
t_h	Hold Time, HIGH or LOW	5.0	2.0	ns	
	$\overline{PE}$ to CP				
t_s	Setup Time,				
	HIGH or LOW	5.0	9.0	ns	
	U/$\overline{D}$ to CP				
t_h	Hold Time, HIGH or LOW	5.0	2.0	ns	
	U/$\overline{D}$ to $\overline{CP}$				
t_w	CP Pulse Width,	5.0	5.0	ns	
	HIGH or LOW				

(1) Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD}	Power Dissipation	60.0	pF	V_{CC} = 5.0V
	Capacitance			

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