54AC175 • 54ACT175 Quad D Flip-Flop

Check for Samples: 54AC175, 54ACT175

FEATURES

- **Edge-triggered D-type inputs**
- **Buffered positive edge-triggered clock**
- **Asynchronous common reset**
- **True and complement output**
- **Outputs source/sink 24 mA**
- **'ACT175 has TTL-compatible inputs**
- **Standard Microcircuit Drawing (SMD)**
  - **—'AC175: 5962-89552**
  - **—'ACT175: 5962-89693**

DESCRIPTION

The 'AC/'ACT175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

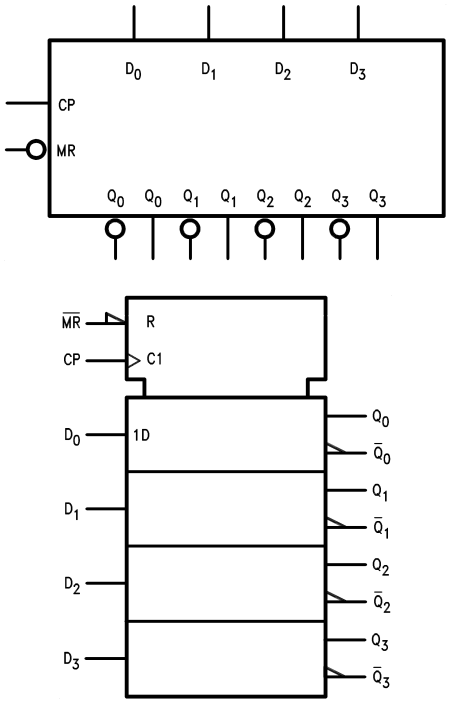


Figure 1. IEEE/IEC

Pin Names	Description
D_0–D_3	Data Inputs
CP	Clock Pulse Input
$\overline{MR}$	Master Reset Input
Q_0–Q_3	True Outputs
$\overline{Q}_0$–$\overline{Q}_3$	Complement Outputs

Connection Diagram

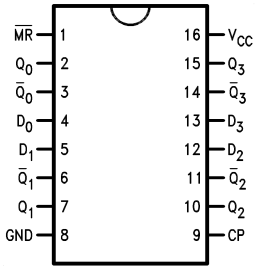


Figure 2. Pin Assignment for DIP and Flatpak

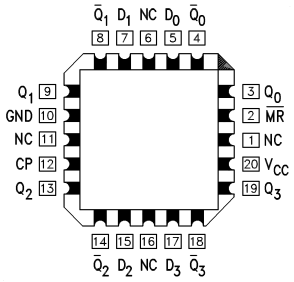


Figure 3. Pin Assignment for LCC

Functional Description

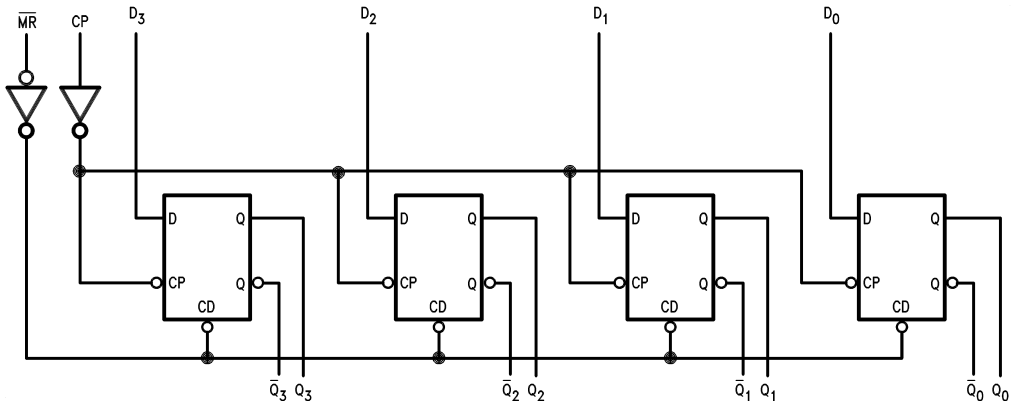
The 'AC/'ACT175 consists of four edge-triggered D flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and $\overline{Q}$ outputs to follow. A LOW input on the Master Reset ($\overline{MR}$) will force all Q outputs LOW and $\overline{Q}$ outputs HIGH independent of Clock or Data inputs. The 'AC/'ACT175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

Truth Table
(1)

Inputs	Outputs	
@ t_n, $\overline{MR}$ = H	@ t_{n+1}	
D_n	Q_n	$\overline{Q}_n$
L	L	H
H	H	L

(1) H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit Time before Clock Pulse
t_{n+1} = Bit Time after Clock Pulse

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source	
or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C

(1) Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

Recommended OperatingConditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt)	
'AC Devices	

Recommended OperatingConditions (continued)

V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

			54AC		
Symbol	**Parameter**	**V_{CC}**	**T_A = −55°C to +125°C**	**Units**	**Conditions**
		(V)	**Guaranteed Limits**		
V_{IH}	Minimum High Level	3.0	2.1		V_{OUT} = 0.1V
	Input Voltage	4.5	3.15	V	or V_{CC} − 0.1V
		5.5	3.85		
V_{IL}	Maximum Low Level	3.0	0.9		V_{OUT} = 0.1V
	Input Voltage	4.5	1.35	V	or V_{CC} − 0.1V
		5.5	1.65		
V_{OH}	Minimum High Level	3.0	2.9		I_{OUT} = −50 µA
	Output Voltage	4.5	4.4	V	
		5.5	5.4		
					(1) V_{IN} = V_{IL} or V_{IH}
		3.0	2.4		I_{OH} = −12 mA
		4.5	3.7	V	I_{OH} = −24 mA
		5.5	4.7		I_{OH} = −24 mA
V_{OL}	Maximum Low Level	3.0	0.1		I_{OUT} = 50 µA
	Output Voltage	4.5	0.1	V	
		5.5	0.1		
					(1) V_{IN} = V_{IL} or V_{IH}
		3.0	0.50		I_{OL} = 12 mA
		4.5	0.50	V	I_{OL} = 24 mA
		5.5	0.50		I_{OL} = 24 mA
I_{IN}	Maximum Input	5.5	±1.0	µA	V_I = V_{CC}, GND
	Leakage Current				
	(2)				
I_{OLD}	Minimum Dynamic	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}	Output Current	5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent	5.5	160.0	µA	V_{IN} = V_{CC}
	Supply Current				or GND

(1) All outputs loaded; thresholds on input associated with output under test.
(2) Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACT Family Devices

			54ACT		
Symbol	**Parameter**	**V_{CC}**	**T_A = −55°C to +125°C**	**Units**	**Conditions**
		(V)	**Guaranteed Limits**		
V_{IH}	Minimum High Level	4.5	2.0	V	V_{OUT} = 0.1V
	Input Voltage	5.5	2.0		or V_{CC} − 0.1V
V_{IL}	Maximum Low Level	4.5	0.8	V	V_{OUT} = 0.1V
	Input Voltage	5.5	0.8		or V_{CC} − 0.1V
V_{OH}	Minimum High Level	4.5	4.4	V	I_{OUT} = −50 µA
	Output Voltage	5.5	5.4		
					(1) V_{IN} = V_{IL} or V_{IH}
		4.5	3.70	V	I_{OH} = −24 mA
		5.5	4.70		I_{OH} = −24 mA
V_{OL}	Maximum Low Level	4.5	0.1	V	I_{OUT} = 50 µA
	Output Voltage	5.5	0.1		
					(1) V_{IN} = V_{IL} or V_{IH}
		4.5	0.50	V	I_{OL} = 24 mA
		5.5	0.50		I_{OL} = 24 mA
I_{IN}	Maximum Input	5.5	±1.0	µA	V_I = V_{CC}, GND
	Leakage Current				
I_{CCT}	Maximum	5.5	1.6	mA	V_I = V_{CC} − 2.1V
	I_{CC}/Input				
	(2)				
I_{OLD}	Minimum Dynamic	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}	Output Current	5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent	5.5	160.0	µA	V_{IN} = V_{CC}
	Supply Current				or GND

(1) All outputs loaded; thresholds on input associated with output under test.
(2) Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

Symbol	Parameter		54AC		Units	Fig. No.
		V_{CC} (V) [1]	T_A = −55°C to +125°C, C_L = 50 pF			
			Min	Max		
f_{max}	Maximum Clock Frequency	3.3	95		MHz	
		5.0	95			
t_{PLH}	Propagation Delay CP to Q_n or $\overline{Q}_n$	3.3	1.0	14.5	ns	
		5.0	1.5	10.5		
t_{PHL}	Propagation Delay CP to Q_n or $\overline{Q}_n$	3.3	1.0	15.0	ns	
		5.0	1.5	11.5		
t_{PLH}	Propagation Delay $\overline{MR}$ to $\overline{Q}_n$	3.3	1.0	15.0	ns	
		5.0	1.5	11.0		
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	3.3	1.0	13.5	ns	
		5.0	1.5	10.5		

(1) Voltage Range 3.3 is 3.3V ±0.3VVoltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter		54AC	Units	
		V_{CC}	T_A = −55°C to +125°C		Fig.
		(V)	C_L = 50 pF		No.
		(1)	Guaranteed Minimum		
t_s	Setup Time, HIGH or LOW	3.3	5.0	ns	
	D_n to CP	5.0	3.5		
t_h	Hold Time, HIGH or LOW	3.3	2.0	ns	
	D_n to CP	5.0	2.5		
t_w	CP Pulse Width	3.3	6.0	ns	
	HIGH or LOW	5.0	5.0		
t_w	$\overline{MR}$ Pulse Width, LOW	3.3	5.5	ns	
		5.0	5.0		
t_{rec}	Recovery Time	3.3	1.5	ns	
	$\overline{MR}$ to CP	5.0	1.5		

(1) Voltage Range 3.3 is 3.3V ±0.3VVoltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter		54ACT		Units	
		V_{CC}	T_A = −55°C to +125°C			Fig.
		(V)	C_L = 50 pF			No.
		(1)	Min	Max		
f_{max}	Maximum Clock	5.0	95		MHz	
	Frequency					
t_{PLH}	Propagation Delay	5.0	1.5	11.5	ns	
	CP to Q_n or $\overline{Q}_n$					
t_{PHL}	Propagation Delay	5.0	1.5	12.5	ns	
	CP to Q_n or $\overline{Q}_n$					
t_{PLH}	Propagation Delay	5.0	1.5	11.5	ns	
	$\overline{MR}$ to $\overline{Q}_n$					
t_{PHL}	Propagation Delay	5.0	1.5	11.0	ns	
	$\overline{MR}$ to Q_n					

(1) Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter		54ACT	Units	
		V_{CC}	T_A = −55°C to +125°C		Fig.
		(V)	C_L = 50 pF		No.
		(1)	Guaranteed Minimum		
t_s (H)	Setup Time	5.0	3.5	ns	
t_s (L)	D_n to CP		3.5		
t_h	Hold Time, HIGH or LOW	5.0	1.5	ns	
	D_n to CP				
t_w	CP Pulse Width	5.0	5.0	ns	
	HIGH or LOW				
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	5.0	ns	
t_{rec}	Recovery Time, $\overline{MR}$ to CP	5.0	1.5	ns	

(1) Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation	45.0	pF	V_{CC} = 5.0V
	Capacitance			

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