

54ACTQ16374

54ACTQ16374 16-Bit D Flip-Flop with TRI-STATE Outputs



Literature Number: SNOS589

54ACTQ16374 16-Bit D Flip-Flop with TRI-STATE® Outputs

General Description

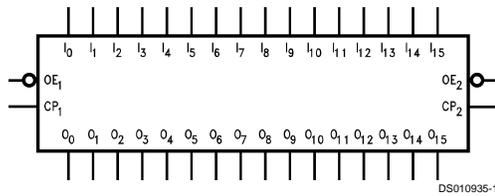
The 'ACTQ16374 contains sixteen non-inverting D flip-flops with TRI-STATE outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and Output Enable (OE) are common to each byte and can be shorted together for full 16-bit operation.

The 'ACTQ16245 utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series® features GTO® output control for superior performance.

Features

- Utilizes NSC FACT Quiet Series technology
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Buffered Positive edge-triggered clock
- Separate control logic for each byte
- 16-bit version of the 'ACTQ374
- Outputs source/sink 24 mA
- Standard Microcircuit Drawing (SMD) 5962-9452801

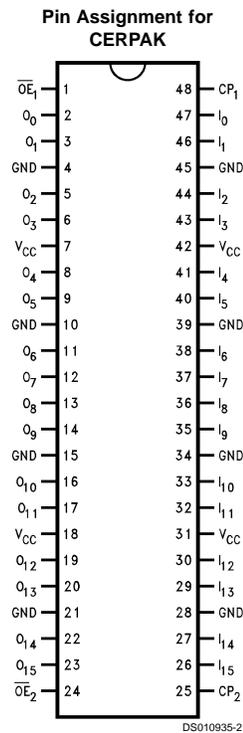
Logic Symbol



Pin Description

Pin Names	Description
\overline{OE}_n	Output Enable Input (Active Low)
CP_n	Clock Pulse Input
I_0-I_{15}	Inputs
O_0-O_{15}	Outputs

Connection Diagram



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Functional Description

The 'ACTQ16374 consists of sixteen edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. Each byte has a buffered clock and buffered Output Enable common to all flip-flops within that byte. The description which follows applies to each byte. Each flip-flop will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP_n) transition. With the Output Enable (\overline{OE}_n) LOW, the contents of the flip-flops are available at the outputs. When \overline{OE}_n is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE}_n input does not affect the state of the flip-flops.

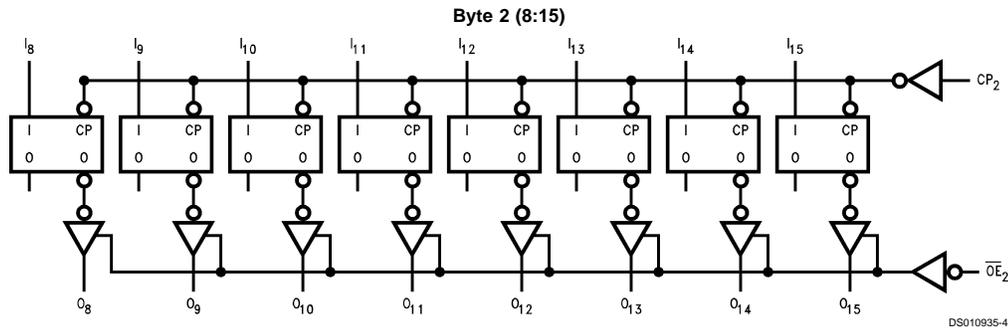
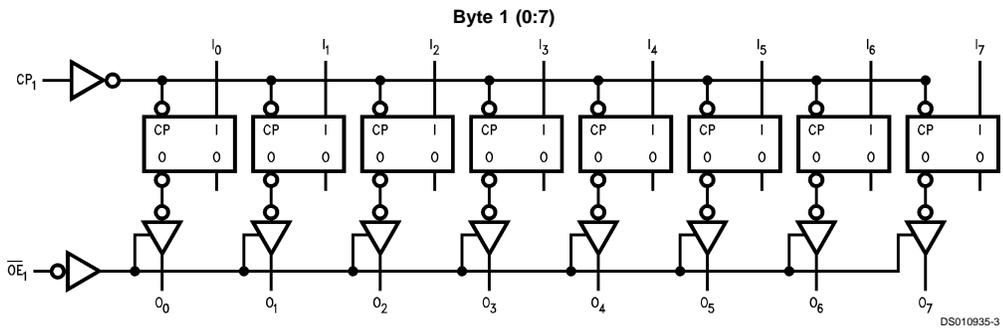
Truth Tables

Inputs			Outputs
CP_1	\overline{OE}_1	I_0-I_7	O_0-O_7
N	L	H	H
N	L	L	L
L	L	X	(Previous)
X	H	X	Z

Inputs			Outputs
CP_2	\overline{OE}_2	I_8-I_{15}	O_8-O_{15}
N	L	H	H
N	L	L	L
L	L	X	(Previous)
X	H	X	Z

H = High Voltage Level
 L = Low Voltage Level
 X = Immaterial
 Z = High Impedance

Logic Diagrams



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source/Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin	±50 mA
Junction Temperature CDIP	+175°C
Storage Temperature	-65°C to +150°C

Recommended Operating Conditions

Supply Voltage (V_{CC}) 'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A): 54ACTQ	-55°C to +125°C
Minimum Input Edge Rate (dV/dt) 'ACTQ Devices	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	54ACTQ	Units	Conditions
			$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$		
			Guaranteed Limits		
V_{IH}	Minimum High Input Voltage	4.5	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	2.0		
V_{IL}	Maximum Low Input Voltage	4.5	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	0.8		
V_{OH}	Minimum High Output Voltage	4.5	4.4	V	$I_{OUT} = -50 \mu A$
		5.5	5.4		
		4.5	3.70	V	(Note 2) $V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
		5.5	4.70		
V_{OL}	Maximum Low Output Voltage	4.5	0.1	V	$I_{OUT} = 50 \mu A$
		5.5	0.1		
		4.5	0.50	V	(Note 2) $V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
		5.5	0.50		
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5	±10.0	µA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, \text{GND}$
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	$V_I = V_{CC}, \text{GND}$
I_{CCT}	Maximum I_{CC} /Input	5.5	1.6	mA	$V_I = V_{CC} - 2.1V$
I_{CC}	Max Quiescent Supply Current	5.5	160.0	µA	$V_{IN} = V_{CC}$ or GND (Note 6)
I_{OLD}	(Note 3) Minimum Dynamic Output Current	5.5	50	mA	$V_{OLD} = 1.65V \text{ Max}$
I_{OHD}	Output Current		50	mA	$V_{OHD} = 3.85V \text{ Min}$
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	0.8	V	(Notes 4, 5)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	-0.8	V	(Notes 4, 5)

DC Electrical Characteristics for 'ACTQ Family Devices (Continued)

Note 2: All outputs loaded; thresholds associated with output under test.

Note 3: Maximum test duration 2.0 ms; one output loaded at a time.

Note 4: Maximum number of outputs that can switch simultaneously is n. (n - 1) outputs are switched LOW and one output held LOW.

Note 5: Maximum number of outputs that can switch simultaneously is n. (n - 1) outputs are switched HIGH and one output held HIGH.

Note 6: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 7)	54ACTQ		Units
			$T_A =$ -55°C to +125°C $C_L = 50$ pF		
			Min	Max	
f_{max}	Maximum Clock Frequency	5.0	65		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to O_n	5.0	3.0	10.5	ns
t_{PZH} t_{PZL}	Output Enable Time	5.0	3.0	10.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time	5.0	2.0	9.0	ns

Note 7: Voltage Range 5.0 is 5.0V \pm 0.5V.

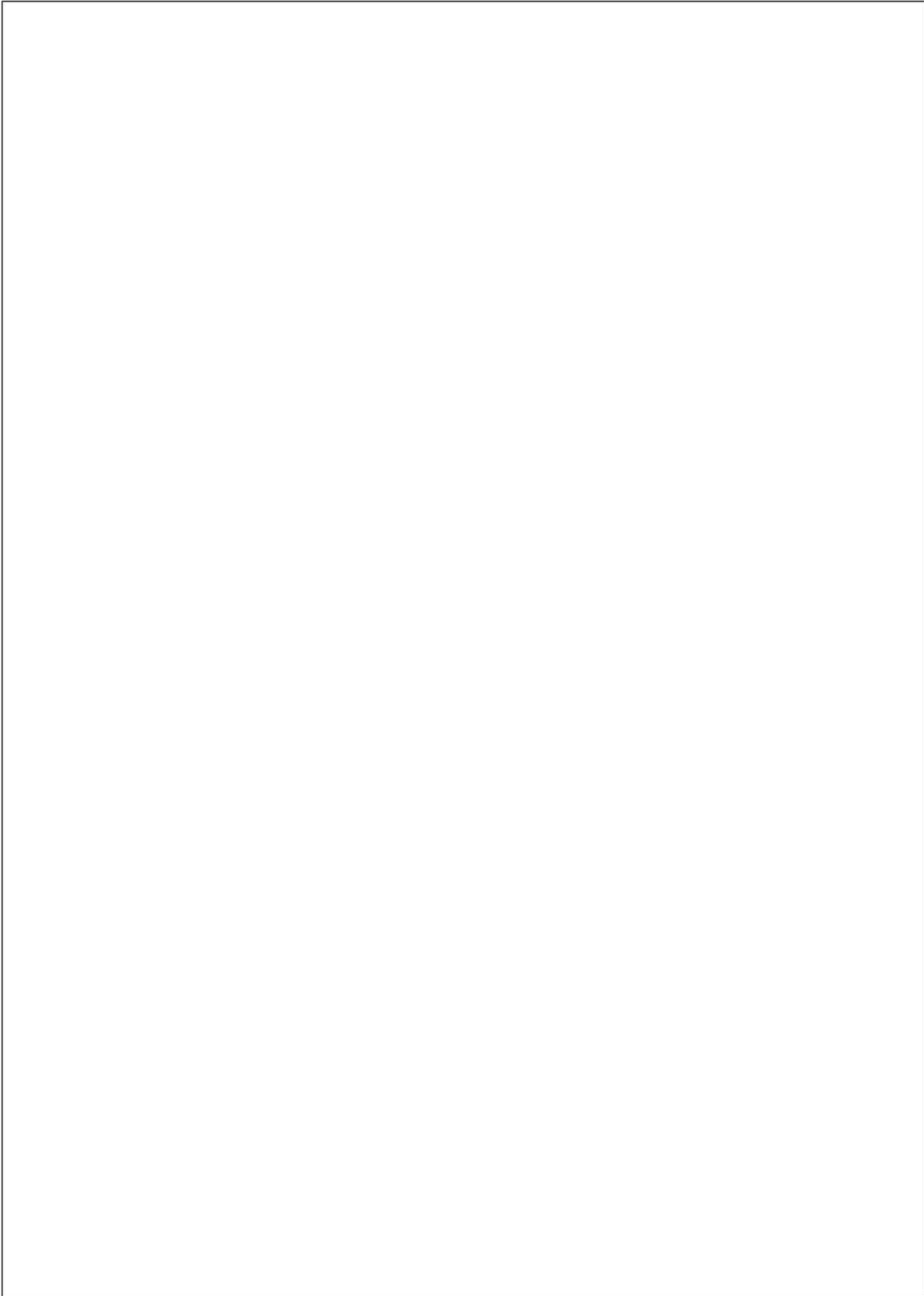
AC Operating Requirements

Symbol	Parameter	V_{CC} (V) (Note 8)	54ACTQ		Units
			$T_A =$ -55°C to +125°C $C_L = 50$ pF		
			Guaranteed Limits		
t_S	Setup Time, HIGH or LOW, Input to Clock	5.0	3.0		ns
t_H	Hold Time, High or LOW, Input to Clock	5.0	1.0		ns
t_W	CP Pulse Width, HIGH or LOW	5.0	5.0		ns

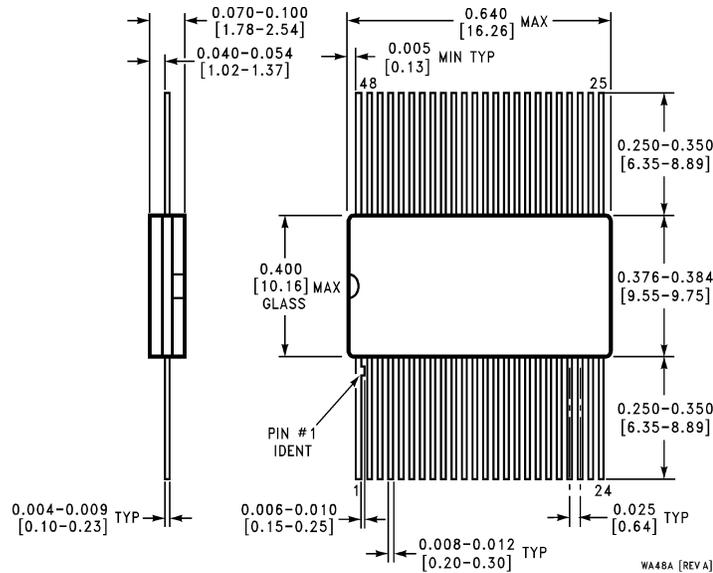
Note 8: Voltage Range 5.0 is 5.0V \pm 0.5V.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation	95	pF	$V_{CC} = 5.0V$



Physical Dimensions inches (millimeters) unless otherwise noted



**48-Lead CERPAK
 NS Package Number WA48A**

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