54FCT374

54FCT374 Octal D-Type Flip-Flop with -TRISTATE Outputs

Literature Number: SNOS428

National Semiconductor

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54FCT374
Octal D-Type Flip-Flop with TRI-STATE® Outputs

General Description

The 'FCT374 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

Features

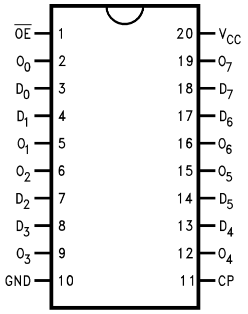
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- TTL input and output level compatible
- Low CMOS power consumption
- Output sink capability of 32 mA, source capability of 12 mA
- Standard Microcircuit Drawing (SMD) 5962-9314901

Ordering Code

Military	Package Number	Package Description
54FCT374DMQB	J20A	20-Lead Ceramic Dual-In-Line
54FCT374FMQB	W20A	20-Lead Cerpack
54FCT374LMQB	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Connection Diagrams

Pin Assignment for DIP and Flatpak



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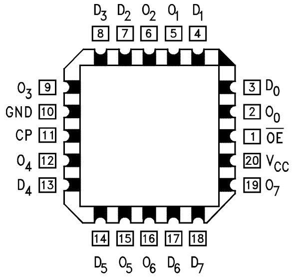
Pin Assignment for LCC



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Pin Descriptions

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)
O_0–O_7	TRI-STATE Outputs

Functional Description

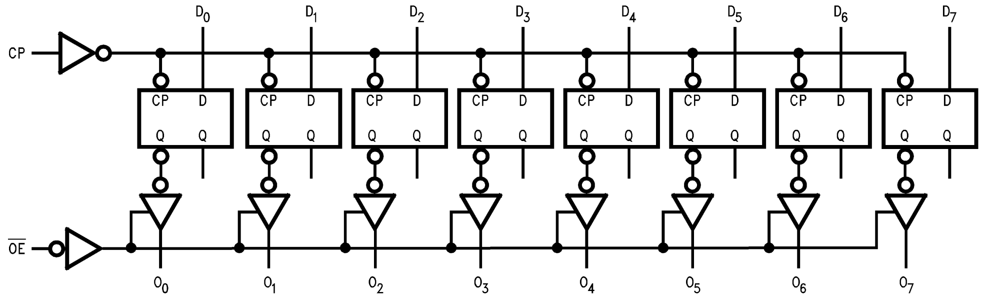
The 'FCT374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs are in a high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	N	L	L	Z	Load
H	N	H	H	Z	Load
L	N	L	L	L	Data Available
L	N	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
N = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65˚C to +150˚C
Ambient Temperature under Bias	−55˚C to +125˚C
Junction Temperature under Bias Ceramic	−55˚C to +175˚C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage	−0.5V to +7.0V
Input Current	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature Military	−55˚C to +125˚C
Supply Voltage Military	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

DC Electrical Characteristics

Symbol	Parameter		FCT374		Units	V_{CC}	Conditions
			Min	Max			
V_{IH}	Input HIGH Voltage		2.0		V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54FCT	4.3		V	Min	I_{OH} = −300 µA
		54FCT	2.4		V	Min	I_{OH} = −12 mA
V_{OL}	Output LOW Voltage	54FCT		0.2	V	Min	I_{OL} = 300 µA
		54FCT		0.5	V	Min	I_{OL} = 32mA
I_{IH}	Input HIGH Current			5 5	µA	Max	V_{IN} = 2.7V (Note 3) V_{IN} = V_{CC}
I_{IL}	Input LOW Current			−5 −5	µA	Max	V_{IN} = 0.5V (Note 3) V_{IN} = 0.0V
I_{OZH}	Output Leakage Current			10	µA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}$ = 2.0V
I_{OZL}	Output Leakage Current			−10	µA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}$ = 2.0V
I_{OS}	Output Short-Circuit Current		−60		mA	Max	V_{OUT} = 0.0V
I_{CCQ}	Power Supply Current			1.5	mA	Max	V_{IN} = 0.2V or V_{IN} = 5.3V, f_I = 0MHz
ΔI_{CC}	Power Supply Current			2.0	mA	Max	V_{IN} = 3.4V
I_{CCT}	Additional I_{CC}/Input			6.0	mA	Max	V_I = V_{CC} − 2.1V or V_{IN} = GND, f_{CP} = 10MHz, Outputs open, $\overline{OE}$ = GND, one bit toggling at f_I = 5MHz, 50% duty cycle
				5.5	mA	Max	V_I = 5.3V or V_{CC} = 0.2V, f_{CP} = 10MHz, Outputs open, $\overline{OE}$ = GND, one bit toggling at f_I = 5MHz, 50% duty cycle
I_{CCD}	Dynamic I_{CC}	No Load		0.4	mA/ MHz	Max	Outputs Open, $\overline{OE}$ = GND, One bit toggling, 50% duty cycle, V_{IN} = 5.3V or V_{IN} = 0.2V

Note 2: For 8-bit toggling, $I_{CCD} < 0.8$ mA/MHz.

Note 3: Guaranteed, but not tested.

AC Electrical Characteristics

Symbol	Parameter	54FCT $T_A = -55°C$ to $+125°C$ $V_{CC} = 4.5V$ to $5.5V$ $C_L = 50$ pF		Units
		Min	Max	
t_{PLH}	Propagation Delay	2.0	11.0	ns
t_{PHL}	CP to O_n	2.0	11.0	
t_{PZH}	Output Enable Time	1.5	14.0	ns
t_{PZL}		1.5	14.0	
t_{PHZ}	Output Disable Time	1.5	8.0	ns
t_{PLZ}		1.5	8.0	

AC Operating Requirements

Symbol	Parameter	54FCT $T_A = -55°C$ to $+125°C$ $V_{CC} = 4.5V$ to $5.5V$ $C_L = 50$ pF		Units
		Min	Max	
$t_s(H)$	Setup Time, HIGH	2.5		ns
$t_s(L)$	or LOW D_n to CP	2.5		
$t_h(H)$	Hold Time, HIGH	2.5		ns
$t_h(L)$	or LOW D_n to CP	2.5		
$t_w(H)$	Pulse Width, CP	7.0		ns
$t_w(L)$	HIGH or LOW	7.0		

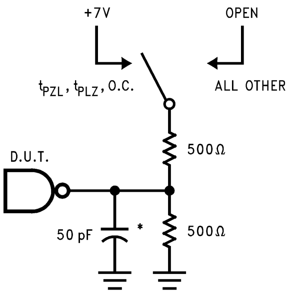
Capacitance

Symbol	Parameter	Typ	Units	Conditions ($T_A = 25°C$)
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0V$
C_{OUT} (Note 4)	Output Capacitance	9.0	pF	$V_{CC} = 5.0V$

Note 4: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

Capacitance (Continued)

AC Loading



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*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

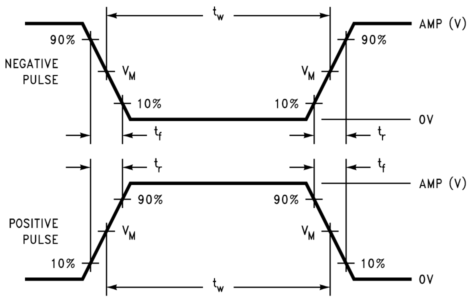

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FIGURE 2. V_M = 1.5V

Input Pulse Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

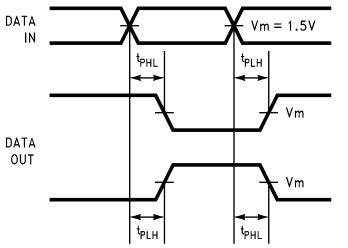

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FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

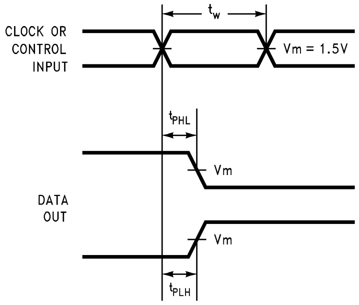

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FIGURE 5. Propagation Delay, Pulse Width Waveforms

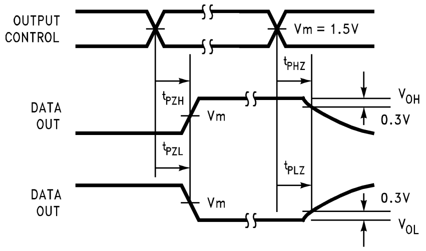

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FIGURE 6. TRI-STATE Output HIGH and LOW Enable and Disable Times

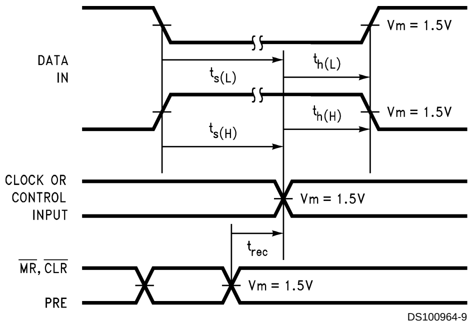

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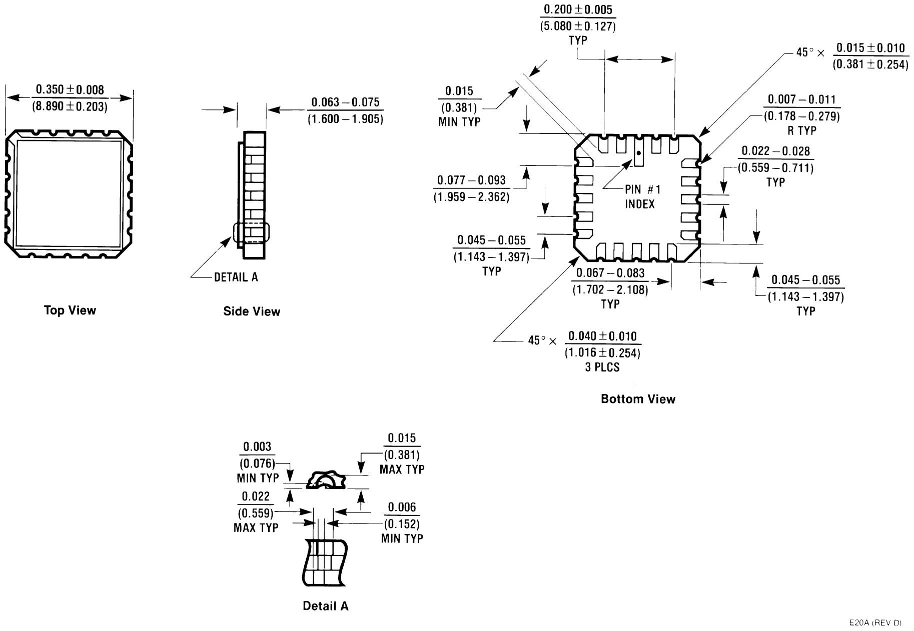
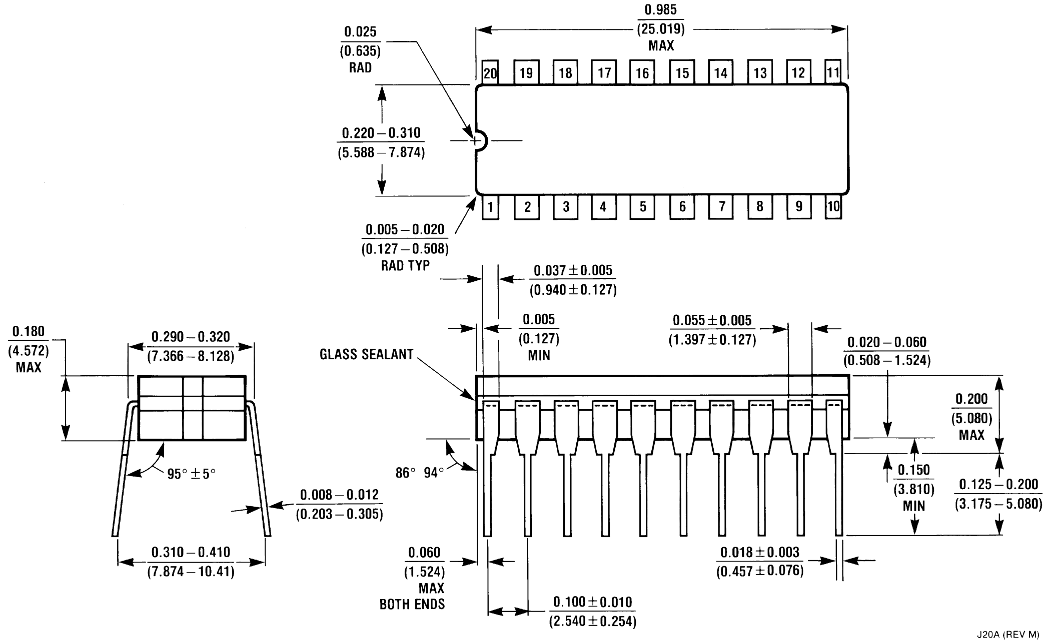
FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

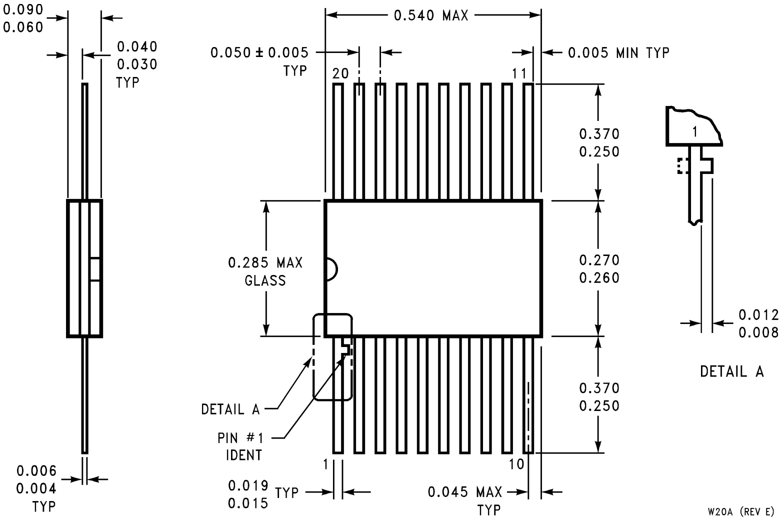


20-Terminal Ceramic Chip Carrier (L)
NS Package Number E20A



20-Lead Ceramic Dual-In-Line (D)
NS Package Number J20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Ceramic Flatpak (F)
NS Package Number W20A

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