54LCX16373

54LCX16373 Low Voltage 16-Bit Transparent Latch with 5V Tolerant Inputs and Outputs



Literature Number: SNOS490A



54LCX16373

Low Voltage 16-Bit Transparent Latch with 5V Tolerant Inputs and Outputs

General Description

The LCX16373 contains sixteen non-inverting latches with TRI-STATE® outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is low, the data that meets the setup time is latched. Data appears on the bus when the Output Enable $(\overline{\text{OE}})$ is LOW. When OE is HIGH, the outputs are in TRI-STATE.

The LCX16373 is designed for low voltage (3.3V) $\rm V_{\rm CC}$ applications with capability of interfacing to a 5V signal environment.

The LCX16373 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V-3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented noise/EMI reduction circuitry
- Functionally compatible with the 54 series 16373
- ESD performance:

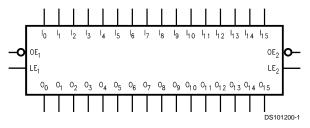
Human body model > 2000V Machine model > 200V

■ Standard Microcircuit Drawing (SMD) 5962-9953401

Ordering Code

| Order Number | Package Number | Package Description |
|-----------------|----------------|--------------------------|
| 54LCX16373W-QML | WA48A | 48-Lead Ceramic Flatpack |

Logic Symbol

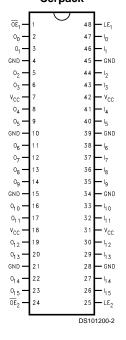


Pin Descriptions

| Pin Names | Description | | |
|---------------------------------|----------------------------------|--|--|
| OE _n | Output Enable Input (Active Low) | | |
| LEn | Latch Enable Input | | |
| I ₀ -I ₁₅ | Inputs | | |
| O ₀ -O ₁₅ | Outputs | | |

Connection Diagram

Pin Assignment for Cerpack



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Functional Description

The LCX16373 contains sixteen D-type latches with TRI-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable (LE_n) input is HIGH, data on the I_n enters the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its I input changes. When LE_n is LOW, the latches store information that was present on the I inputs a setup time preceding the HIGH-to-LOW transition of LE_n. The TRI-STATE standard outputs are controlled by the Output Enable (\overline{OE}_n) input. When \overline{OE}_n is LOW, the standard outputs are in the 2-state mode. When $\overline{\text{OE}}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

| Inputs | | | Outputs |
|------------------------------------|---|--------------------------------|----------------|
| LE_1 \overline{OE}_1 I_0-I_7 | | O ₀ -O ₇ | |
| X | Н | Χ | Z |
| Н | L | L | L |
| Н | L | Н | Н |
| L | L | X | O _o |

| Inputs | | | Outputs |
|-----------------|-----|---------------------------------|---------------------------------|
| LE ₂ | ŌE₂ | I ₈ -I ₁₅ | O ₈ -O ₁₅ |
| Х | Н | X | Z |
| Н | L | L | L |
| Н | L | Н | Н |
| L | L | X | O _o |

H = High Voltage Level

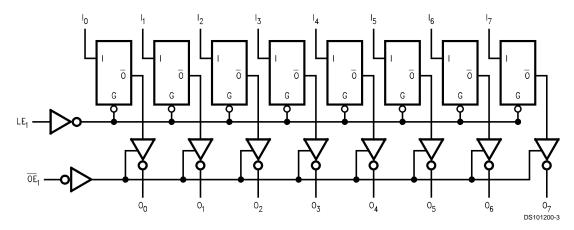
L = Low Voltage Level

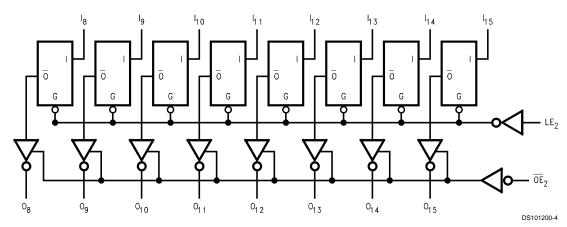
X = Immaterial

Z = High Impedance

O₀ = Previous O₀ before HIGH to LOW transition of Latch Enable

Logic Diagrams





Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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Absolute Maximum Ratings (Note 1)

 $\begin{array}{lll} \mbox{Supply Voltage (V$_{\rm CC}$)} & -0.5\mbox{V to } +7.0\mbox{V} \\ \mbox{DC Input Voltage (V$_{\rm I}$)} & -0.5\mbox{V to } +7.0\mbox{V} \end{array}$

DC Input Diode Current (IIK)

 $V_1 < GND$ –50 mA

DC Output Diode Current (IOK)

 $V_{O} < GND$ -50mA $V_{O} \ge V_{CC}$ +50mA

DC Output Voltage (V_O) (Note 2)

Output in High or Low State -0.5V to $V_{\rm CC}$ + 0.5V Output in TRI-STATE -0.5V to 7.0V

DC Output Source or Sink Current

±50mA

DC V_{CC} or Ground Current ±400mA

Storage Temperature Range

 (T_{STG}) $-65^{\circ}C$ to $+150^{\circ}C$ Power Dissapation 750mW

Junction Temperature (T_J) 175°C

Recommended Operating Conditions (Note 3)

Supply Voltage (V_{CC})

Operating 2.7V to 3.6V Data Retention 1.5V to 3.6V Input Voltage (V_1) 0V to 5.5V

Output Voltage (V_O)

Operating Temperature (T_A) $-55^{\circ}C$ to +125 $^{\circ}C$

Minimum Input Edge Rate (Δt/ΔV)

 V_{IN} from 0.8V to 2.0V, $V_{CC} = 3.0V$ Ons/V to 10ns/V

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Note 3: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

| Symbol | Parameter | Conditions | V _{cc} | $T_A = -55^{\circ}C \text{ to } +125^{\circ}C$ | | Units |
|------------------|---------------------------------------|------------------------------|-----------------|--|------|-------|
| | | | (V) | Min | Max | |
| V _{IH} | HIGH Level Input Voltage | | 2.7-3.6 | 2.0 | | V |
| V _{IL} | LOW Level Input Voltage | | 2.7-3.6 | | 0.8 | V |
| V _{OH} | HIGH Level Output Voltage | I _{OH} = -100 μA | 2.7-3.6 | V _{CC} - 0.2 | | V |
| | | I _{OH} = -12 mA | 2.7 | 2.2 | | V |
| | | I _{OH} = -12 mA | 3.0 | 2.4 | | V |
| | | $I_{OH} = -24 \text{ mA}$ | 3.0 | 2.2 | | V |
| V _{OL} | LOW Level Output Voltage | I _{OL} = 100 μA | 2.7-3.6 | | 0.2 | V |
| | | I _{OL} = 12 mA | 2.7 | | 0.4 | V |
| | | I _{OL} = 24 mA | 3.0 | | 0.55 | V |
| I _I | Input Leakage Current | $0 \le V_1 \le 5.5V$ | 2.7-3.6 | | ±5.0 | μΑ |
| l _{oz} | TRI-STATE Output Leakage | $0 \le V_O \le 5.5V$ | 2.7-3.6 | | ±5.0 | μΑ |
| | | $V_I = V_{IH}$ or V_{IL} | | | | |
| I _{OFF} | Power-Off Leakage Current | V_I or $V_O = 5.5V$ | 0 | | 10 | μΑ |
| I _{cc} | Quiescent Supply Current | $V_I = V_{CC}$ or GND | 2.7-3.6 | | 20 | μΑ |
| | | $3.6V \le V_I, V_O \le 5.5V$ | 2.7-3.6 | | ±20 | μΑ |
| ΔI_{CC} | Increase in I _{CC} per Input | $V_{IH} = V_{CC} - 0.6V$ | 2.7-3.6 | | 500 | μA |

AC Electrical Characteristics

| Symbol | Parameter | $T_A = -55^{\circ}C$ to +125°C, $C_L = 50$ pF, $R_L = 500\Omega$ | | | | Units |
|-------------------|----------------------------------|--|------------|-----------------|--------|-------|
| | | V _{CC} = 3 | .3V ± 0.3V | V _{cc} | = 2.7V | |
| | | Min | Max | Min | Max | |
| t _{PHL} | Propagation Delay | 1.0 | 6.0 | 1.5 | 6.5 | ns |
| t _{PLH} | I _n to O _n | 1.0 | 6.0 | 1.5 | 6.5 | |
| t _{PHL} | Propagation Delay | 1.0 | 6.5 | 1.5 | 7.0 | ns |
| t _{PLH} | LE to O _n | 1.0 | 6.5 | 1.5 | 7.0 | |
| t _{PZL} | Output Enable Time | 1.0 | 6.5 | 1.5 | 7.0 | ns |
| t _{PZH} | | 1.0 | 6.5 | 1.5 | 7.0 | |
| t _{PLZ} | Output Disable Time | 1.0 | 6.5 | 1.5 | 7.0 | ns |
| t _{PHZ} | | 1.0 | 6.5 | 1.5 | 7.0 | |
| t _S | Setup Time, In to LE | 2.5 | | 2.5 | | ns |
| t _H | Hold Time, I _n to LE | 2.0 | | 2.0 | | ns |
| t _{vv} | LE Pulse Width | 3.5 | | 3.5 | | ns |
| t _{OSHL} | Output to Output Skew (Note 4) | | 1.0 | | 1.0 | ns |
| toslh | | | 1.0 | | 1.0 | |

Note 4: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics

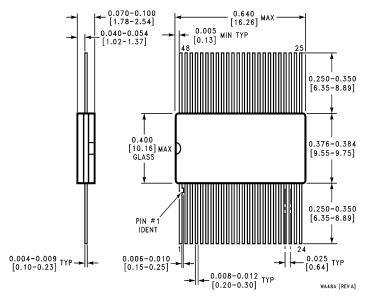
| Symbol | Parameter | Conditions | V _{cc} | T _A = 25°C Max | Units |
|------------------|---|---|-----------------|------------------------------|-------|
| V _{OLP} | Quiet Output Dynamic Peak V _{OL} | $C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$ | 3.3 | 1.2 | V |
| V _{OLV} | Quiet Output Dynamic Valley V _{OL} | $C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$ | 3.3 | -1.1 | V |

Capacitance

| Symbol | Parameter | Conditions | Max | Units |
|------------------|-------------------------------|---|-----|-------|
| C _{IN} | Input Capacitance | V_{CC} = Open, V_{I} = 0V or V_{CC} | 10 | pF |
| C _{OUT} | Output Capacitance | $V_{CC} = 3.3V$, $V_{I} = 0V$ or V_{CC} | 12 | pF |
| C _{PD} | Power Dissipation Capacitance | $V_{CC} = 3.3V$, $V_{I} = 0V$ or V_{CC} , $f = 10$ MHz | 40 | pF |

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Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead Ceramic Flatpack Package Number WA48A

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