54/74157 54S/74S157 54LS/74LS157

QUAD 2-INPUT MULTIPLEXER

S 1 16 Vcc

10a 2 15 Ē

11d 3 14 loc

Za 4 13 l1c

10b 5 12 Zc

11b 6 11 lod

10 I1d

9 Z₀

CONNECTION DIAGRAM
PINOUT A

LOGIC SYMBOL

GND 8

V_{CC} = Pin 16 GND = Pin 8

DESCRIPTION — The '157 is a high speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four buffered outputs present the selected data in the true (non-inverted) form. The '157 can also be used to generate any four of the 16 different functions to two variables.

ORDERING CODE: See Section 9

	PIN	COMMERCIAL GRADE	MILITARY GRADE	PKG	
PKGS	оит	$V_{CC} = +5.0 \text{ V } \pm 5\%,$ $T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$	$V_{CC} = +5.0 \text{ V} \pm 10\%,$ $T_A = -55^{\circ}\text{C to} + 125^{\circ}\text{C}$	TYPE	
Plastic DIP (P)	Α	74157PC, 74S157PC 74LS157PC		9B	
Ceramic DIP (D)	Α	74157DC, 74S157DC 74LS157DC	54157DM, 54S157DM 54LS157DM	6B	
Flatpak (F)	Α	74157FC, 74S157FC 74LS157FC	54157FM, 54S157FM 54LS157FM	4L	

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

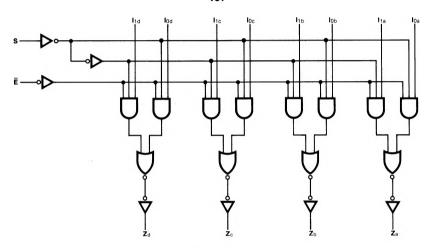
PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW	
I _{0a} — I _{0d}	Source 0 Data Inputs	1.0/1.0	1.25/1.25	0.5/0.25	
l _{1a} — l _{1d}	Source 1 Data Inputs	1.0/1.0	1.25/1.25	0.5/0.25	
Ē	Enable Input (Active LOW)	1.0/1.0	2.5/2.5	1.0/0.5	
S	Select Input	1.0/1.0	2.5/2.5	1.0/0.5	
$Z_a - Z_d$	Outputs	20/10	25/12.5	10/5.0 (2.5)	

FUNCTIONAL DESCRIPTION — The '157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input (E) is active LOW. When E is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The '157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

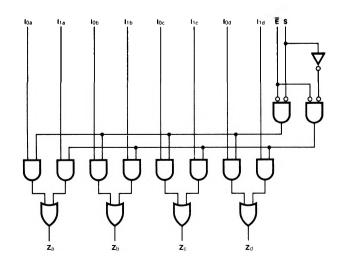
$$\begin{split} Z_a &= \overline{E} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S}) \\ Z_c &= \overline{E} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S}) \end{split} \qquad \begin{aligned} Z_b &= \overline{E} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S}) \\ Z_d &= \overline{E} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S}) \end{aligned}$$

A common use of the '157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The '157 can generate any four of the 16 different functions of two variables with one variable common. This is useful for implementing highly irregular logic.

LOGIC DIAGRAMS '157



'S157 • 'LS157



TRUTH TABLE

	INP	UTS	OUTPUT	
Ē	S	Z		
Н	Х	Х	Х	L
L	н	Х	L	L
L	н	Х	н	н
L	L	L	Х	L
L	L	Н	Х	н

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74		54/74\$		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max			
los	Output Short Circuit Current	XM XC	-20 -18	-55 -55	-40 -40	-100 -100	-20 -20	-100 -100	mA	V _{CC} = Max
lcc	Power Supply Current			48		78		16	mA	V _{CC} = Max All Inputs = 4.5 V

AC CHARACTERISTICS: $V_{CC} = +5.0 \text{ V}$, $T_A = +25^{\circ}\text{C}$ (See Section 3 for waveforms and load configurations)

		54/74	54/74\$	54/74LS	UNITS	CONDITIONS
SYMBOL	PARAMETER		$C_L = 15 pF$ $R_L = 280 \Omega$			
		Min Max	Min Max	Min Max		
tpLH tpHL	Propagation Delay S to Z _n	23 27	15 15	26 24	ns	Figs. 3-1, 3-20
tpLH tpHL	Propagation Delay E to Z _n	20 21	12.5 12	20 21	ns	Figs. 3-1, 3-4
tpLH tpHL	Propagation Delay In to Zn	14 14	7.5 6.5	14 14	ns	Figs. 3-1, 3-5