

54LS/74LS322

8-BIT SERIAL/PARALLEL REGISTER

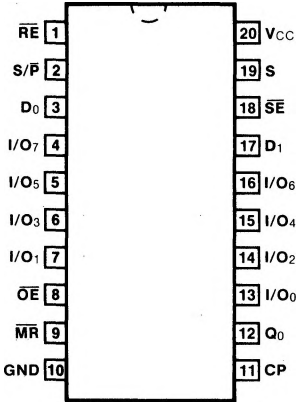
(With Sign Extend)

DESCRIPTION — The '322 is an 8-bit shift register with provision for either serial or parallel loading and with 3-state parallel outputs plus a bi-state serial output. Parallel data inputs and parallel outputs are multiplexed to minimize pin count. State changes are initiated by the rising edge of the clock. Four synchronous modes of operation are possible: hold (store), shift right with serial entry, shift right with sign extend and parallel load. An asynchronous Master Reset (**MR**) input overrides clocked operation and clears the register. The '322 is specifically designed for operation with the '384 Multiplier and provides the sign extend function required for the '384.

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V _{CC} = +5.0 V ±5%, T _A = 0° C to +70° C	V _{CC} = +5.0 V ±10%, T _A = -55° C to +125° C	
Plastic DIP (P)	A	74LS322PC		9Z
Ceramic DIP (D)	A	74LS322DC	54LS322DM	4E
Flatpak (F)	A	74LS322FC	54LS322FM	4F

CONNECTION DIAGRAM
PINOUT A

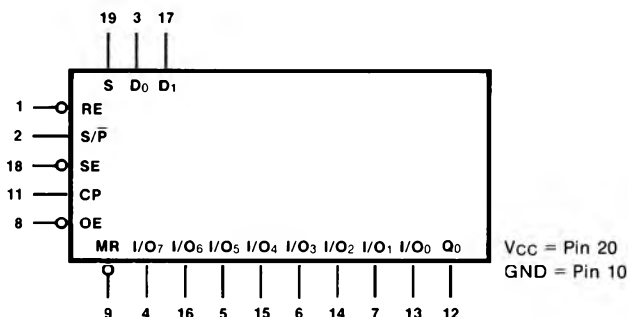


INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

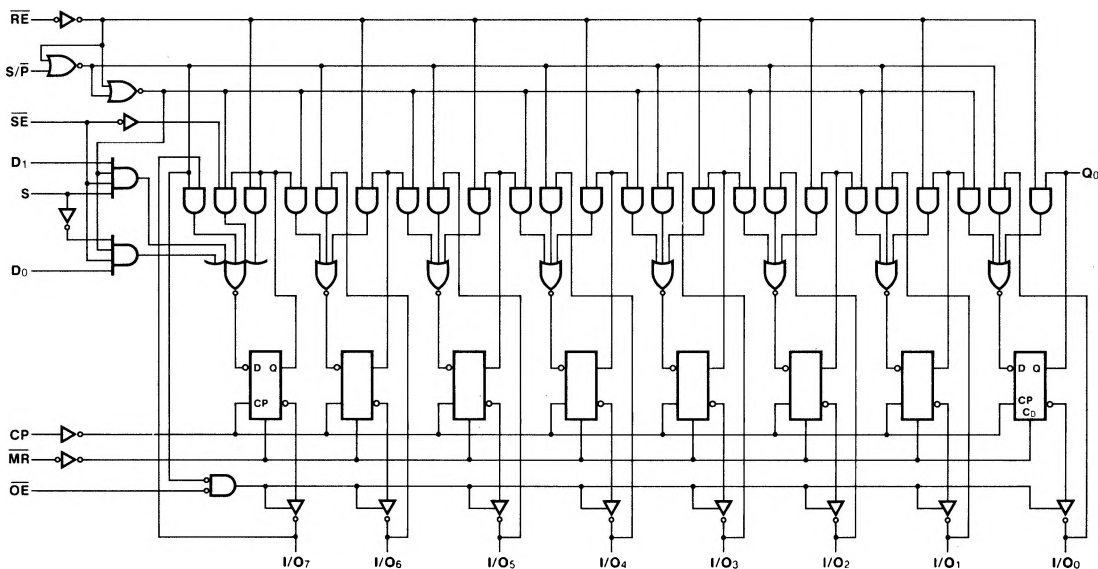
PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
RE	Register Enable Input (Active LOW)	0.5/0.23
S/P	Serial (HIGH) or Parallel (LOW) Mode Control Input	0.5/0.23
SE	Sign Extend Input (Active LOW)	1.5/0.68
S	Serial Data Select Input	1.0/0.45
D ₀ , D ₁	Serial Data Inputs	0.5/0.23
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.23
MR	Asynchronous Master Reset Input (Active LOW)	0.5/0.23
OE	3-State Output Enable Input (Active LOW)	0.5/0.23
Q ₀	Bi-State Serial Output	11/5.0 (2.5)
I/O ₀ — I/O ₇	Multiplexed Parallel Inputs or 3-State Parallel Outputs	0.5/0.23 65/5.0 (25)/(2.5)

FUNCTIONAL DESCRIPTION — The '322 contains eight D-type edge triggered flip-flops and the interstage gating required to perform right shift and the intrastage gating necessary for hold and synchronous parallel load operations. A LOW signal on $\overline{RE}$ enables shifting or parallel loading, while a HIGH signal enables the hold mode. A HIGH signal on $S/\overline{P}$ enables shift right, while a LOW signal disables the 3-state output buffers and enables parallel loading. In the shift right mode a HIGH signal on $\overline{SE}$ enables serial entry from either D_0 or D_1 , as determined by the S input. A LOW signal on $\overline{SE}$ enables shift right but Q_7 reloads its contents, thus performing the sign extend function required for the '384 Two's Complement Multiplier. A HIGH signal on $\overline{OE}$ disables the 3-state output buffers, regardless of the other control inputs. In this condition the shifting and loading operations can still be performed.

LOGIC SYMBOL



LOGIC DIAGRAM



MODE TABLE

MODE	INPUTS							OUTPUTS								Q ₀
	MR	RE	S/ $\overline{P}$	$\overline{S}$ E	S	$\overline{O}E^*$	CP	I/O ₇	I/O ₆	I/O ₅	I/O ₄	I/O ₃	I/O ₂	I/O ₁	I/O ₀	
Clear	L	X	X	X	X	L	X	L	L	L	L	L	L	L	L	L
	L	X	X	X	X	H	X	Z	Z	Z	Z	Z	Z	Z	Z	L
Parallel Load	H	L	L	X	X	X	$\int$	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	I ₀
Shift Right	H	L	H	H	L	L	$\int$	D ₀	O ₇	O ₆	O ₅	O ₄	O ₃	O ₂	O ₁	O ₁
	H	L	H	H	H	L	$\int$	D ₁	O ₇	O ₆	O ₅	O ₄	O ₃	O ₂	O ₁	O ₁
Sign Extend	H	L	H	L	X	L	$\int$	O ₇	O ₇	O ₆	O ₅	O ₄	O ₃	O ₂	O ₁	O ₁
Hold	H	H	X	X	X	L	$\int$	NC	NC	NC	NC	NC	NC	NC	NC	NC

*When the $\overline{O}E$ input is HIGH, all I/O_n terminals are at the high-impedance state; sequential operation or clearing of the register is not affected.

1. I₇ — I₀ = The level of the steady-state input at the respective I/O terminal is loaded into the flip-flop while the flip-flop outputs (except Q₀) are isolated from the I/O terminal.

2. D₀, D₁ = The level of the steady-state inputs to the serial multiplexer input.

3. O₇ — O₀ = The level of the respective Q_n flip-flop prior to the last Clock LOW-to-HIGH transition.

NC = No Change Z = High-Impedance Output State H = HIGH Voltage Level L = LOW Voltage Level

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I _{CC}	Power Supply Current		60	mA	V _{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		C _L = 15 pF			
		Min	Max		
f _{max}	Maximum Clock Frequency	35		MHz	Figs. 3-1, 3-8
t _{PLH} t _{PHL}	Propagation Delay CP to I/O _n	23 25		ns	
t _{PLH} t _{PHL}	Propagation Delay CP to Q ₀	25 29		ns	Figs. 3-1, 3-16
t _{PHL}	Propagation Delay MR to I/O _n	33		ns	
t _{PHL}	Propagation Delay MR to Q ₀	30		ns	
t _{PZH} t _{PZL}	Output Enable Time OE to I/O _n	18 23		ns	Figs. 3-3, 3-11, 3-12 R _L = 2 kΩ
t _{PHZ} t _{PLZ}	Output Disable Time OE to I/O _n	15 15		ns	Figs. 3-3, 3-11, 3-12 R _L = 2 kΩ, C _L = 5 pF
t _{PZH} t _{PZL}	Output Enable Time S/P to I/O _n	25 30		ns	Figs. 3-3, 3-11, 3-12 R _L = 2 kΩ
t _{PHZ} t _{PLZ}	Output Disable Time S/P to I/O _n	23 23		ns	Figs. 3-3, 3-11, 3-12 R _L = 2 kΩ, C _L = 5 pF

AC OPERATING REQUIREMENTS: $V_{CC} = +5.0\text{ V}$, $T_A = +25^\circ\text{C}$

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{RE}$ to CP	24 24		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{RE}$ to CP	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW D_0 , D_1 or I/O_n to CP	10 10		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW D_0 , D_1 or I/O_n to CP	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{SE}$ to CP	15 15		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{SE}$ to CP	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW $S/\overline{P}$ to CP	24 24		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW S to CP	15 15		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW S or $S/\overline{P}$ to CP	0 0		ns	
t_w (H)	CP Pulse Width HIGH	15		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width LOW	15		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{MR}$ to CP	15		ns	