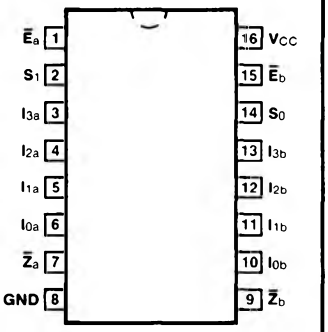
54LS/74LS352

DUAL 4-INPUT MULTIPLEXER

DESCRIPTION — The '352 is a very high speed dual 4-input multiplexer with Common Select inputs and individual Enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the inverted (complementary) form. The '352 is the functional equivalent of the '153 except with inverted outputs.

- **INVERTED VERSION OF THE '153**
- **SEPARATE ENABLES FOR EACH MULTIPLEXER**
- **INPUT CLAMP DIODE LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

CONNECTION DIAGRAM
PINOUT A



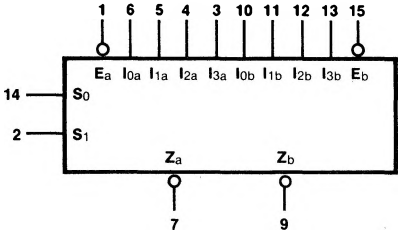
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74LS352PC		9B
Ceramic DIP (D)	A	74LS352DC	54LS352DM	6B
Flatpak (F)	A	74LS352FC	54LS352FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
I_{0a} — I_{3a}	Side A Data Inputs	0.5/0.25
I_{0b} — I_{3b}	Side B Data Inputs	0.5/0.25
S_0, S_1	Common Select Inputs	0.5/0.25
$\overline{E}_a$	Side A Enable Input (Active LOW)	0.5/0.25
$\overline{E}_b$	Side B Enable Input (Active LOW)	0.5/0.25
$\overline{Z}_a$, $\overline{Z}_b$	Multiplexer Outputs (Inverted)	10/5.0 (2.5)

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — The '352 is a dual 4-input multiplexer. It selects two bits of data from up to four sources under the control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs ($\overline{Z}_a$, $\overline{Z}_b$) are forced HIGH.

The logic equations for the outputs are shown below.

$$\overline{Z}_a = \overline{\overline{E}_a \bullet (I_{0a} \bullet S_1 \bullet S_0 + I_{1a} \bullet S_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet S_0 + I_{3a} \bullet S_1 \bullet S_0)}$$

$$\overline{Z}_b = \overline{\overline{E}_b \bullet (I_{0b} \bullet S_1 \bullet S_0 + I_{1b} \bullet S_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet S_0 + I_{3b} \bullet S_1 \bullet S_0)}$$

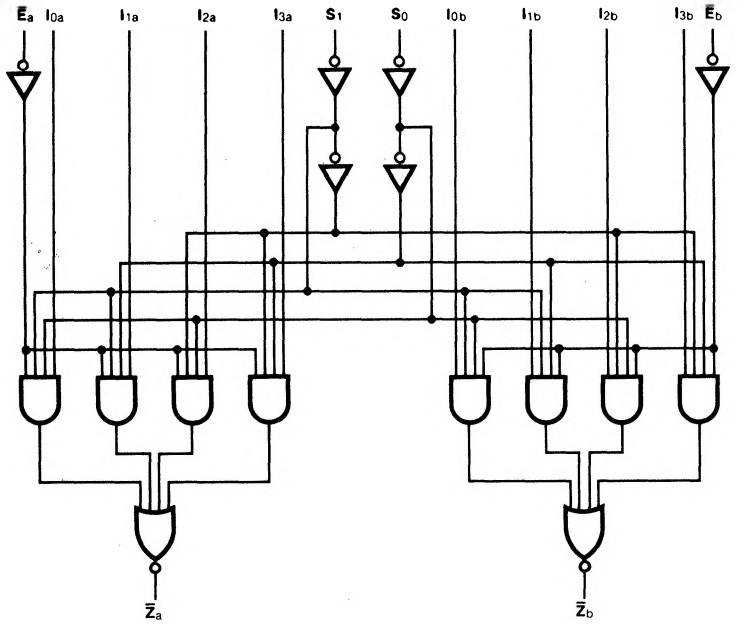
The '352 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select inputs. A less obvious application is a function generator. The '352 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

TRUTH TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	$\overline{Z}$
X	X	H	X	X	X	X	H
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
H	L	L	X	L	X	X	H
H	L	L	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
H	H	L	X	X	X	L	H
H	H	L	X	X	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		10	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{Z}_n$		22 38	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_n$ to $\overline{Z}_n$		15 20	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$		12 12	ns	Figs. 3-1, 3-4