

54LS/74LS374

OCTAL D-TYPE FLIP-FLOP

(With 3-State Outputs)

DESCRIPTION — The '374 is a high speed, low power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (\overline{OE}) is common to all flip-flops. The '374 is manufactured using advanced low power Schottky technology and is compatible with all Fairchild TTL families.

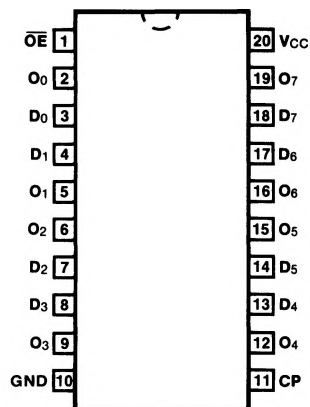
- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED POSITIVE EDGE-TRIGGERED CLOCK**
- **3-STATE OUTPUTS FOR BUS ORIENTED APPLICATIONS**

ORDERING CODE: See Section 9

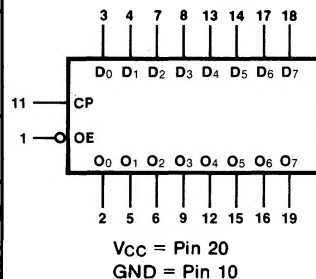
| PKGS | PIN OUT | COMMERCIAL GRADE | MILITARY GRADE | PKG TYPE |
|-----------------|---------|---|---|----------|
| | | $V_{CC} = +5.0\text{ V} \pm 5\%$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$ | $V_{CC} = +5.0\text{ V} \pm 10\%$, $T_A = -55^\circ\text{C to } +125^\circ\text{C}$ | |
| Plastic DIP (P) | A | 74LS374PC | | 9Z |
| Ceramic DIP (D) | A | 74LS374DC | 54LS374DM | 4E |
| Flatpak (F) | A | 74LS374FC | 54LS374FM | 4F |

CONNECTION DIAGRAM

PINOUT A



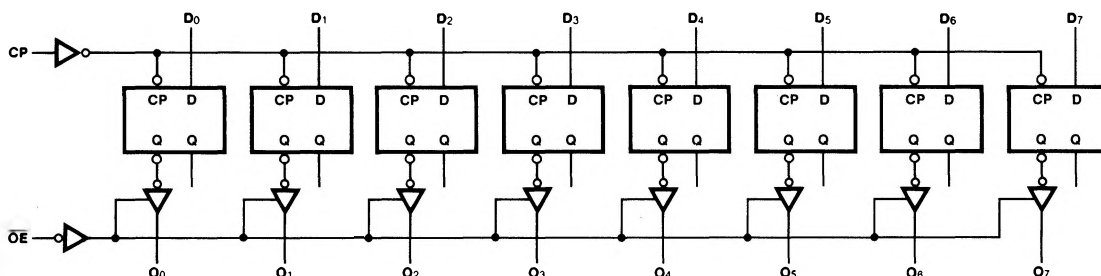
LOGIC SYMBOL



INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions



| PIN NAMES | DESCRIPTION | 54/74LS (U.L.) HIGH/LOW |
|-----------------|--|----------------------------|
| $D_0 - D_7$ | Data Inputs | 0.5/0.25 |
| CP | Clock Pulse Input (Active Rising Edge) | 0.5/0.25 |
| \overline{OE} | 3-State Output Enable Input (Active LOW) | 0.5/0.25 |
| $O_0 - O_7$ | 3-State Outputs | 65/15 (25)/(7.5) |

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION — The '374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable (\overline{OE}) LOW, the contents of the eight flip-flops are available at the outputs. When the \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

TRUTH TABLE

| INPUTS | | OUTPUTS | |
|----------------|---|---------|----------------|
| D _n | CP | OE | O _n |
| H |  | L | H |
| L |  | L | L |
| X | X | H | Z |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| SYMBOL | PARAMETER | 54/74LS | | UNITS | CONDITIONS |
|-----------------|-----------------------------------|---------|-----|-------|--|
| | | Min | Max | | |
| I _{CC} | Power Supply Current, Outputs OFF | | 45 | mA | V _{CC} = Max, D _n = Gnd \overline{OE} = 4.5 V |

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

| SYMBOL | PARAMETER | 54/74LS | | UNITS | CONDITIONS |
|--------------------------------------|---|------------------------|----------|-------|--|
| | | C _L = 45 pF | | | |
| | | Min | Max | | |
| f _{max} | Maximum Clock Frequency | 35 | | MHz | Figs. 3-1, 3-8 |
| t _{PLH} t _{PHL} | Propagation Delay CP to O _n | | 28 28 | ns | Figs. 3-1, 3-8 |
| t _{PZH} t _{PZL} | Output Enable Time | | 28 28 | ns | Figs. 3-3, 3-11, 3-12 R _L = 667 Ω |
| t _{PHZ} t _{PLZ} | Output Disable Time | | 20 25 | ns | Figs. 3-3, 3-11, 3-12 R _L = 667 Ω, C _L = 5 pF |

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

| SYMBOL | PARAMETER | 54/74LS | | UNITS | CONDITIONS |
|--|--|----------|-----|-------|------------|
| | | Min | Max | | |
| t _s (H) t _s (L) | Setup Time HIGH or LOW D _n to CP | 20 20 | | ns | Fig. 3-6 |
| t _h (H) t _h (L) | Hold Time HIGH or LOW D _n to CP | 0 0 | | ns | |
| t _w (H) t _w (L) | CP Pulse Width HIGH or LOW | 15 15 | | ns | Fig. 3-8 |