

54LS/74LS490

DUAL DECADE COUNTER

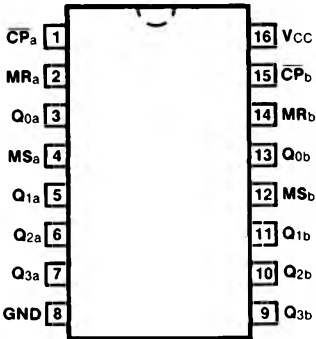
DESCRIPTION —The '490 contains a pair of high speed 4-stage ripple counters. Each half of the '490 has individual Clock, Master Reset and Master Set (Preset 9) inputs. Each section counts in the 8421 BCD code.

- **DUAL VERSION OF 54LS/74LS90**
- **INDIVIDUAL ASYNCHRONOUS CLEAR AND PRESET TO 9 FOR EACH COUNTER**
- **COUNT FREQUENCY—TYPICALLY 65 MHz**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **TTL AND CMOS COMPATIBLE**

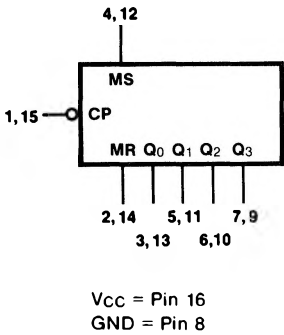
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0\text{ V} \pm 5\%$, $T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$	$V_{CC} = +5.0\text{ V} \pm 10\%$, $T_A = -55^{\circ}\text{C to } +125^{\circ}\text{C}$	
Plastic DIP (P)	A	74LS490PC		9B
Ceramic DIP (D)	A	74LS490DC	54LS490DM	6B
Flatpak (F)	A	74LS490FC	54LS490FM	4L

CONNECTION DIAGRAM
PINOUT A



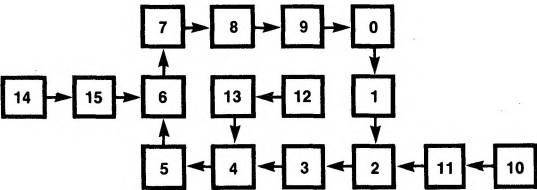
LOGIC SYMBOL



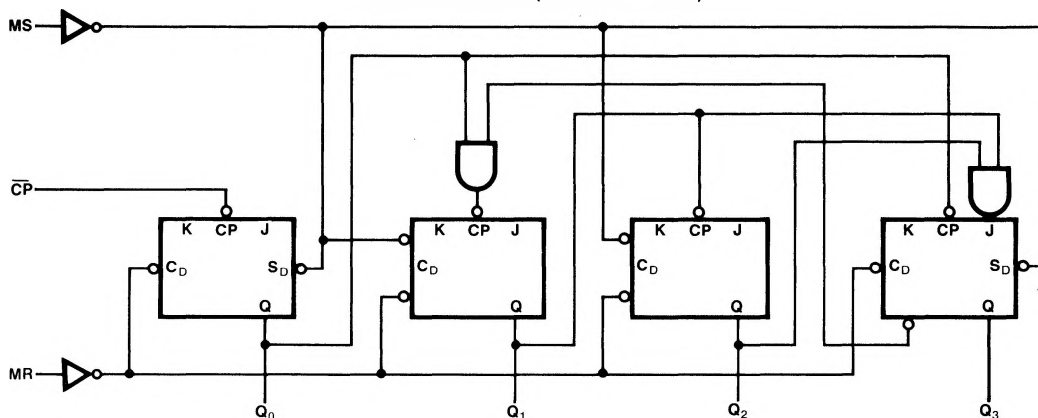
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
MS	Master Set (Set to 9) Input (Active HIGH)	0.5/0.25
MR	Master Reset Input (Active HIGH)	0.5/0.25
CP	Clock Pulse Input (Active Falling Edge)	1.5/1.5
Q ₀ — Q ₃	Counter Outputs	10/5.0 (2.5)

STATE DIAGRAM



LOGIC DIAGRAM (one half shown)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		26	mA	$V_{CC} = \text{Max}$

AC CHARACTERISTICS: $V_{CC} = +5.0 \text{ V}$, $T_A = +25^\circ\text{C}$ (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		$C_L = 15 \text{ pF}$			
		Min	Max		
f_{max}	Maximum Count Frequency	40		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0	15 15		ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay CP to Q_1 or Q_3	30 30		ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay CP to Q_2	45 45		ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay MS to Q_n	35 35		ns	Figs. 3-1, 3-17
t_{PHL}	Propagation Delay MR to Q_n	39		ns	Figs. 3-1, 3-17

AC OPERATING REQUIREMENTS: $V_{CC} = +5.0 \text{ V}$, $T_A = +25^\circ\text{C}$

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
$t_w \text{ (H)}$	$\overline{\text{CP}}$ Pulse Width HIGH	20		ns	Fig. 3-9
$t_w \text{ (H)}$	MR, MS Pulse Width HIGH	20		ns	Fig. 3-17
t_{rec}	Recovery Time, MR or MS to $\overline{\text{CP}}$	15		ns	Fig. 3-17