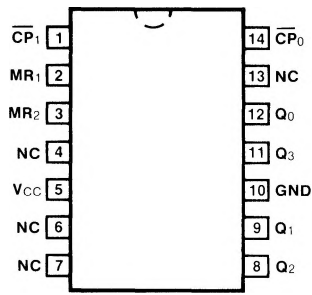


54/7493A
54LS/74LS93
DIVIDE-BY-SIXTEEN COUNTER

CONNECTION DIAGRAM
PINOUT A

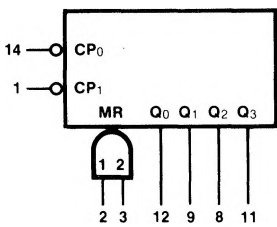


DESCRIPTION — The '93 is a 4-stage ripple counter containing a high speed flip-flop acting as a divide-by-two and three flip-flops connected as a divide-by-eight. HIGH signals on the Master Reset (MR) inputs override the clocks and force all outputs to the LOW state.

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		VCC = +5.0 V $\pm$ 5%, TA = 0°C to +70°C	VCC = +5.0 V $\pm$ 10%, TA = -55°C to +125°C	
Plastic DIP (P)	A	7493APC, 74LS93PC		9A
Ceramic DIP (D)	A	7493ADC, 74LS93DC	5493ADM, 54LS93DM	6A
Flatpak (F)	A	7493AFC, 74LS93FC	5493AFM, 54LS93FM	3I

LOGIC SYMBOL



VCC = Pin 5
GND = Pin 10
NC = Pins 4, 6, 7, 13

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
CP ₀	$\div$ 2 Section Clock Input (Active Falling Edge)	2.0/2.0	1.0/1.5
CP ₁	$\div$ 5 Section Clock Input (Active Falling Edge)	2.0/2.0	1.0/1.0
MR ₁ , MR ₂	Asynchronous Master Reset Inputs (Active HIGH)	1.0/1.0	0.5/0.25
Q ₀	$\div$ 2 Section Output*	20/10	10/5.0 (2.5)
Q ₁ — Q ₃	$\div$ 8 Section Outputs	20/10	10/5.0 (2.5)

*The Q₀ output is guaranteed to drive the full rated fan-out plus the CP₁ input.

FUNCTIONAL DESCRIPTION — The '93 is a 4-bit ripple type binary counter. It consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output of each device is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input of the device. A gated AND asynchronous Master Reset (MR_1 , MR_2) is provided which overrides the clocks and resets (clears) all the flip-flops. Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes.

- A. 4-Bit Ripple Counter — The output Q_0 must be externally connected to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous divisions of 2, 4, 8, and 16 are performed at the Q_0 , Q_1 , Q_2 , and Q_3 outputs as shown in the Truth Table.
- B. 3-Bit Ripple Counter — The input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1 , Q_2 , and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

MODE SELECTION

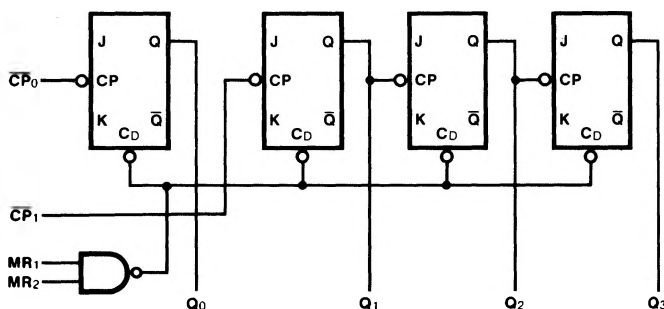
RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = HIGH Voltage Level
L = LOW Voltage Level

TRUTH TABLE

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

NOTE: Output Q_0 connected to $\overline{CP}_1$.

LOGIC DIAGRAM

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{IH}	Input HIGH Current $\overline{CP}_0$ or $\overline{CP}_1$		1.0		0.2	mA	$V_{CC} = \text{Max}$, $V_{IN} = 5.5 \text{ V}$
I_{CC}	Power Supply Current		39		15	mA	$V_{CC} = \text{Max}$

AC CHARACTERISTICS: $V_{CC} = +5.0 \text{ V}$, $T_A = +25^\circ \text{ C}$ (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		C _L = 15 pF R _L = 400 Ω		C _L = 15 pF			
		Min	Max	Min	Max		
f _{max}	Maximum Count Frequency CP ₀ Input	32		32		MHz	Figs. 3-1, 3-9
f _{max}	Maximum Count Frequency CP ₁ Input	16		16		MHz	Figs. 3-1, 3-9
t _{PLH} t _{PHL}	Propagation Delay CP ₀ to Q ₀	16 18		16 18		ns	Figs. 3-1, 3-9
t _{PLH} t _{PHL}	Propagation Delay CP ₀ to Q ₃	70 70		70 70		ns	Figs. 3-1, 3-9
t _{PLH} t _{PHL}	Propagation Delay CP ₁ to Q ₁	16 21		16 21		ns	Figs. 3-1, 3-9
t _{PLH} t _{PHL}	Propagation Delay CP ₁ to Q ₂	32 35		32 35		ns	Figs. 3-1, 3-9
t _{PLH} t _{PHL}	Propagation Delay CP ₁ to Q ₃	51 51		51 51		ns	Figs. 3-1, 3-9
t _{PHL}	Propagation Delay MR to Q _n	40		40		ns	Figs. 3-1, 3-17

AC OPERATING REQUIREMENTS: $V_{CC} = +5.0 \text{ V}$, $T_A = +25^\circ \text{ C}$

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
$t_w (H)$	$\overline{CP}_0$ Pulse Width HIGH		15		15	ns	Fig. 3-9
$t_w (H)$	$\overline{CP}_1$ Pulse Width HIGH		30		30	ns	Fig. 3-9
$t_w (H)$	MR Pulse Width HIGH		15		15	ns	Fig. 3-17
t_{rec}	Recovery Time, MR to $\overline{CP}$		25		25	ns	Fig. 3-17