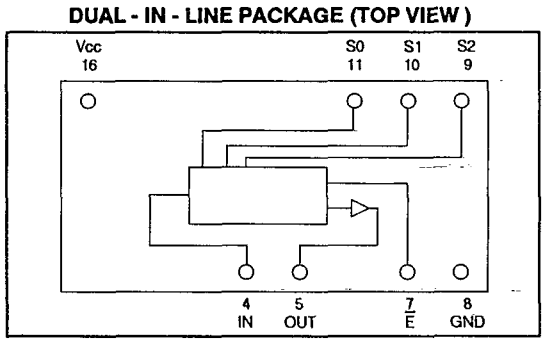
# DIGITAL DELAY MODULES 60A Series
## 3 Bit Programmable 16 Pin Moulded DIP

- ❒ Schottky TTL buffered
- ❒ 8 incremental delays
- ❒ 16 pin package
- ❒ Low profile
- ❒ TTL compatible

DUAL - IN - LINE PACKAGE (TOP VIEW)




### description

The 60A series of 3 Bit Programmable Digital Delay Modules are Schottky TTL buffered delay lines providing eight equal incremental delay steps acting between the input and output. Three input select pins S0, S1 and S2 are used to programme the desired delay and an output enable pin E is active low. The input select pins S0, S1, S2 and the output enable pin E are all standard Schottky logic input compatible. The delay input at pin 4 requires a higher drive such as a dedicated TTL output. See specification table over. The output is directly TTL compatible and the module is a 16 pin dual-in-line configuration having an industry standard pin-out.Internal termination of the delay line is incorporated so that additional external components are not required. These modules are particularly suitable as precision adjustable delays.

### absolute maximum ratings over operating free-air temperature range

| | |
|---|---|
| Supply voltage $V_{cc}$ | .7V |
| Input voltage | .5.5V |
| Min. pulse width as % of total delay | .50% |
| Input pulse repetition rate PRR | 3 x pulse width min. |
| Output rise time | 6ns |
| Operating free-air temperature range | 0C to 70C |
| Storage temperature range | .–55C to 125C |
| Temperature coefficient of delay | ±500ppm/C |
| Lead temperature 1.5mm from case for 10 seconds | 300C |

### drive capabilities

| | |
|---|---|
| Logic 0 output | 20 TTL loads |
| Logic 1 output | 20 TTL loads |

**electrical specifications over operating free-air temperature range**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IH}$ High-level input voltage | | 2 | | | V |
| $V_{IL}$ Low-level input voltage | | | | 0.8 | V |
| $V_{OH}$ High-level output voltage | $V_{IH}$ =2V, $I_{OH}$=–0.8mA $V_{CC}$ =4.75V | 2.4 | 3.4 | | V |
| $V_{OL}$ Low-level output voltage | $V_{CC}$ =4.75V $I_{OL}$=16mA,$V_{IL}$ =0.8V | | 0.2 | 0.4 | V |
| $I_{CC}$ Supply current Inputs all high outputs all open | $V_{CC}$=5.25V $V_{IH}$ = 4.5V | | 29 | 48 | mA |

Note: The input is an unbuffered LC network connection and should be driven from a dedicated TTL buffer such as 74AS04 or similar.

**delay characteristics Vcc = 5V, Ta = 25C, no load at output; input test pulse voltage of 3.2V, pulse width 100% of total delay, rise time 3ns.**

delay tolerance from input to tap ±2ns or ±5% whichever is greater

**60A SERIES 16 Pin DIP**
**Package style J with pins 1, 2, 3, 6, 12, 13, 14, and 15 missing**

| PART No | ZERO STEP (ns) | TOTAL DELAY (ns) ±5% (1) | PER STEP (ns) | PART No | ZERO STEP (ns) | TOTAL DELAY (ns) ±5% (1) | PER STEP (ns) |
|---|---|---|---|---|---|---|---|
| 60A - 014 | 7 ± 2 | 14 | 1 ± 0.5 | 60A - 056 | 7 ± 2 | 56 | 7 ± 1.4 |
| 60A - 021 | | 21 | 2 ± 0.6 | 60A - 063 | | 63 | 8 ± 1.6 |
| 60A - 028 | | 28 | 3 ± 0.7 | 60A - 070 | | 70 | 9 ± 1.8 |
| 60A - 035 | | 35 | 4 ± 0.8 | 60A - 077 | | 77 | 10 ± 2.0 |
| 60A - 042 | | 42 | 5 ± 1.0 | 60A - 084 | | 84 | 11 ± 2.0 |
| 60A - 049 | | 49 | 6 ± 1.2 | 60A - 091 | | 91 | 12 ± 2.0 |

Note: Delays measured at 1.5V on leading edge, Rise Time measured from 0.75V to 2.4V
(1) or ±2ns whichever is greater.

## Function table

| ENABLE | ADDRESS | | | DELAY OUT |
|---|---|---|---|---|
| $\overline{E}$ | S2 | S1 | S0 | |
| H | X | X | X | L |
| L | L | L | L | T0 |
| L | L | L | H | T1 |
| L | L | H | L | T2 |
| L | L | H | H | T3 |
| L | H | L | L | T4 |
| L | H | L | H | T5 |
| L | H | H | L | T6 |
| L | H | H | H | T7 |