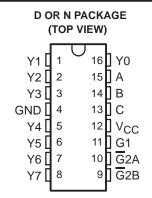
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- Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems
- Noninverting Version of 'ACT11138
- Incorporates 3 Enable Inputs to Simplify Cascading and/or Data Reception
- Inputs Are TTL-Voltage Compatible
- Flow-Through Architecture Optimizes
   PCB Layout
- Center-Pin V<sub>CC</sub> and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs



## description

The 74ACT11238 circuit is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The 74ACT11238 is characterized for operation from – 40°C to 85°C.

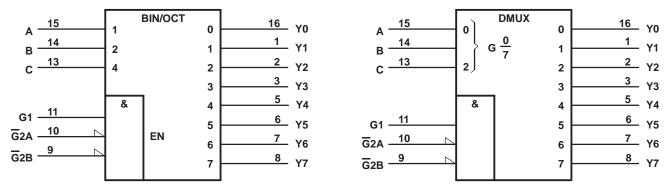
#### **FUNCTION TABLE**

	ENABLE INPUTS			SELECT INPUTS					оиті	PUTS			
G1	G2A	G <sub>2</sub> B	С	В	Α	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
Х	Н	Х	Х	Χ	Χ	L	L	L	L	L	L	L	L
Х	X	Н	Х	X	Χ	L	L	L	L	L	L	L	L
L	X	X	Х	X	Χ	L	L	L	L	L	L	L	L
Н	L	L	L	L	L	Н	L	L	L	L	L	L	L
Н	L	L	L	L	Н	L	Н	L	L	L	L	L	L
Н	L	L	L	Н	L	L	L	Н	L	L	L	L	L
Н	L	L	L	Н	Н	L	L	L	Н	L	L	L	L
Н	L	L	Н	L	L	L	L	L	L	Н	L	L	L
Н	L	L	Н	L	Н	L	L	L	L	L	Н	L	L
Н	L	L	Н	Н	L	L	L	L	L	L	L	Н	L
Н	L	L	Н	Н	Н	L	L	L	L	L	L	L	Н

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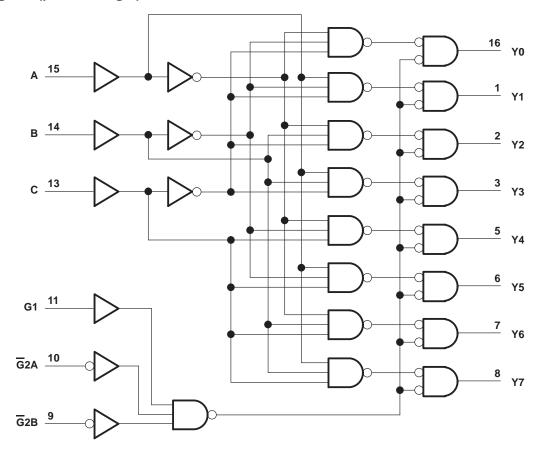
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## logic symbols (alternatives)†



<sup>†</sup> These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



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# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to V <sub>CC</sub> + 0.5 V
Output voltage range, VO (see Note 1)	0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub> )	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	
Continuous current through V <sub>CC</sub> or GND	±200 mA
Storage temperature range	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

		NOM	NOM	MAX	UNIT
Vcc	Supply voltage	4.5		5.5	V
VIH	High-level input voltage	2			V
VIL	Low-level input voltage			0.8	V
VI	Input voltage	0		VCC	V
Vo	Output voltage	0		VCC	V
lOH	High-level output current			-24	mA
l <sub>OL</sub>	Low-level output current			24	mA
Δt/Δν	Input transition rise or fall rate	0		10	ns/V
TA	Operating free-air temperature	- 40		85	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

54544555	TEGT COMPLETIONS	.,	T <sub>A</sub> = 25°C					
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	UNIT
	50 A	4.5 V	4.4			4.4		
	I <sub>OH</sub> = - 50 μA	5.5 V	5.4			5.4		
Voн	Jan. 24 mA	4.5 V	3.94			3.8		V
	I <sub>OH</sub> = – 24 mA	5.5 V	4.94			4.8		
	$I_{OH} = -75 \text{ mA}^{\ddagger}$	5.5 V				3.85		
	I 50 A	4.5 V			0.1		0.1	 
	I <sub>OL</sub> = 50 μA	5.5 V			0.1		0.1	
VoL	24 = 4	4.5 V			0.36		0.44	V
	I <sub>OL</sub> = 24 mA	5.5 V			0.36		0.44	
	$I_{OL} = 75 \text{ mA}^{\ddagger}$	5.5 V					1.65	
IĮ	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 0.1	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		40	mA
∆l <sub>CC</sub> §	$V_I = V_{CC}$ or GND	5.5 V			0.9		1	mA
C <sub>i</sub>	$V_I = V_{CC}$ or GND	5 V		3.5	·		·	pF

<sup>‡</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.



NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>§</sup> This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to VCC.

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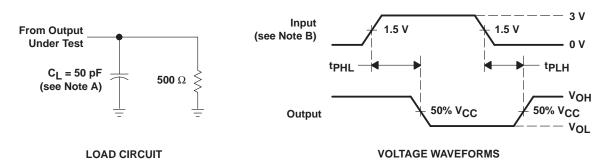
# switching characteristics, $V_{\mbox{\footnotesize CC}}$ = 5 V $\pm$ 0.5 V (see Figure 1)

DADAMETED	FROM	то	T <sub>A</sub> = 25°C			BAINI	MAY	LINUT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	UNIT
t <sub>PLH</sub>	A D an C	V	1.5	5	8.6	1.5	9.6	ns
<sup>t</sup> PHL	A, B or C	Ť	1.5	5.7	9.7	1.5	10.8	
<sup>t</sup> PLH	0.4	V	1.5	6	8.4	1.5	9.4	
<sup>t</sup> PHL	G1	Y	1.5	6.9	10.2	1.5	11.4	ns
<sup>t</sup> PLH	<u> </u>	V	1.5	5.9	9	1.5	10.1	
t <sub>PHL</sub>	GZA, GZB	Y	1.5	7.8	10.7	1.5	12.1	ns

# operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per gate	$C_L = 50 \text{ pF}, \qquad f = 1 \text{ MHz}$	57	pF

## PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \ \Omega$ ,  $t_f = 3 \ ns$ ,  $t_f = 3 \ ns$ .
- C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## **TYPICAL APPLICATION DATA**

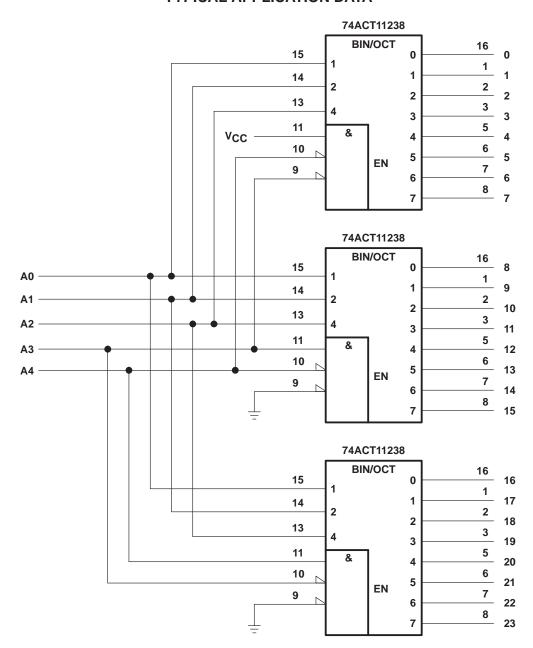


Figure 2. 24-Bit Decoding Scheme

#### **TYPICAL APPLICATION DATA** 74ACT11238 BIN/OCT A0 -A1 -A2 -& VCC -A3 -ΕN A4 -74ACT11238 BIN/OCT & ΕN 74ACT11238 BIN/OCT & ΕN 74ACT11238 BIN/OCT ΕN

Figure 3. 32-Bit Decoding Scheme







i.com 24-Jun-2005

### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
74ACT11238D	OBSOLETE	SOIC	D	16	TBD	Call TI	Call TI
74ACT11238DR	OBSOLETE	SOIC	D	16	TBD	Call TI	Call TI
74ACT11238DR	OBSOLETE	SOIC	D	16	TBD	Call TI	Call TI
74ACT11238N	OBSOLETE	PDIP	N	16	TBD	Call TI	Call TI
74ACT11238N	OBSOLETE	PDIP	N	16	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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