

54ACQ/74ACQ273 • 54ACTQ/74ACTQ273 Quiet Series Octal D Flip-Flop

General Description

The 'AC/'ACT273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

The 'ACQ/'ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic

The information for the ACQ273 is Advanced Information only.

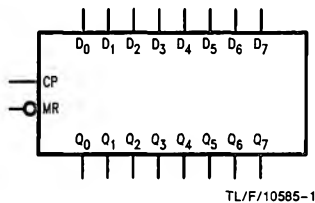
threshold performance. FACT Quiet Series™ features GTOT™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

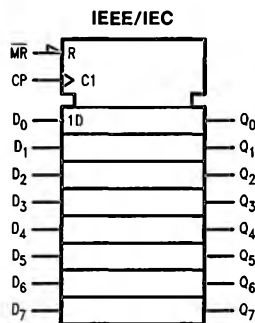
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- Buffered common clock and asynchronous master reset
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'AC/'ACT273
- 4 kV minimum ESD immunity

Ordering Code: See Section 8

Logic Symbols



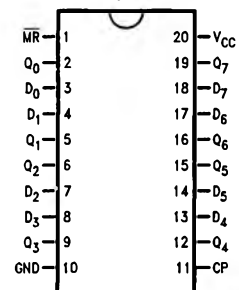
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Connection Diagrams

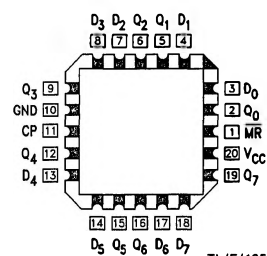
Pin Assignment for DIP, Flatpak and SOIC



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Pin Names	Description
D ₀ -D ₇	Data Inputs
$\overline{MR}$	Master Reset
CP	Clock Pulse Input
Q ₀ -Q ₇	Data Outputs

Pin Assignment for LCC



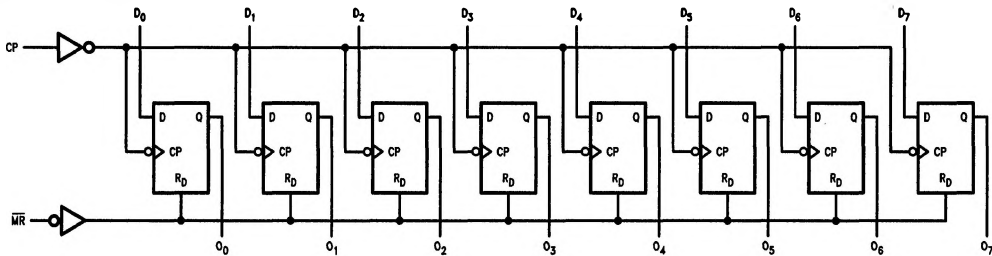
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Mode Select-Function Table

Operating Mode	Inputs			Outputs
	MR	CP	D _n	Q _n
Reset (Clear)	L	X	X	L
Load '1'	H	↗	H	H
Load '0'	H	↘	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW-to-HIGH Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 6.0V
'ACQ	4.5V to 5.5V
'ACTQ	0V to V_{CC}
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACQ/ACTQ	−40°C to +85°C
54ACQ/ACTQ	−55°C to +125°C
Minimum Input Edge Rate $\Delta V/\Delta t$	
'ACQ Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate $\Delta V/\Delta t$	
'ACTQ Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V _{CC} (V)	74ACTQ		54ACTQ		74ACTQ		Units	Conditions
			T _A = +25°C		T _A = −55°C to +125°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits						
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0		2.0		V	V _{OUT} = 0.1V or V _{CC} − 0.1V
		5.5	1.5	2.0	2.0		2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8		0.8		V	V _{OUT} = 0.1V or V _{CC} − 0.1V
		5.5	1.5	0.8	0.8		0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4		4.4		V	I _{OUT} = −50 μA
		5.5	5.49	5.4	5.4		5.4			
		4.5		3.86	3.7		3.76		V	*V _{IN} = V _{IL} or V _{IH} I _{OH} − 24 mA
		5.5		4.86	4.7		4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1		0.1		V	I _{OUT} = 50 μA
		5.5	0.001	0.1	0.1		0.1			
		4.5		0.36	0.50		0.44		V	*V _{IN} = V _{IL} or V _{IH} I _{OL} − 24 mA
		5.5		0.36	0.50		0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0		±1.0		μA	V _I = V _{CC} , GND
I _{CCT}	Maximum I _{CC} /Input	5.5	0.6		1.6		1.5		mA	V _I = V _{CC} − 2.1V

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V _{CC} (V)	74ACTQ		54ACTQ		74ACTQ		Units	Conditions
			T _A = +25°C		T _A = –55°C to +125°C		T _A = –40°C to +85°C			
			Typ	Guaranteed Limits						
I _{OLD}	†Minimum Dynamic Output Current	5.5			50		75		mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5			–50		–75		mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0		80.0		μA	V _{IN} = V _{CC} or GND (Note 1)
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	5.0	1.1	1.5					V	Figures 1, 2 (Notes 2, 3)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	5.0	–0.6	–1.2					V	Figures 1, 2 (Notes 2, 3)
V _{IHD}	Maximum High Level Dynamic Input Voltage	5.0	1.9	2.2					V	(Notes 2, 4)
V _{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8					V	(Notes 2, 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). n – 1 Data inputs are driven 0V to 3V; one output @ GND.

Note 4: Max number of Data Inputs (n) switching. (n – 1) Inputs switching 0V to 3V (†ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}) f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V _{CC} * (V)	74ACTQ			54ACTQ		74ACTQ		Units	Fig No.
			T _A = +25°C C _L = 50 pF			T _A = –55°C to +125°C C _L = 50 pF		T _A = –40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
f _{max}	Maximum Clock Frequency	5.0	125	189		85		110		MHz	
t _{PHL} , t _{PLH}	Propagation Delay Clock to Output	5.0	1.5	6.5	8.5	1.5	10.0	1.5	9.0	ns	2-3, 4
t _{PHL}	Propagation Delay MR to Output	5.0	1.5	7.0	9.0	1.5	11.0	1.5	9.5	ns	2-3, 4
t _{OSHL} , t _{OSLH}	Output to Output Skew** Data to Output	5.0		0.5	1.0				1.0	ns	

*Voltage Range 5.0 is 5.0V ±0.5V.

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V _{CC} * (V)	74ACTQ		54ACTQ	74ACTQ	Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = −55°C to +125°C C _L = 50 pF	T _A = −40°C to +85°C C _L = 50 pF		
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW Data to CP	5.0	1.0	3.5	5.0	3.5	ns	2-7
t _h	Hold Time, HIGH or LOW Data to CP	5.0	−0.5	1.5	2.0	1.5	ns	2-7
t _w	Clock Pulse Width HIGH or LOW	5.0	2.0	4.0	5.0	4.0	ns	2-3
t _w	MR Pulse Width HIGH or LOW	5.0	1.5	4.0	5.0	4.0	ns	2-3
t _{rec}	Recovery Time MR to CP	5.0	0.5	3.0		3.0	ns	2-3, 7

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0V
C _{PD}	Power Dissipation Capacitance	40.0	pF	V _{CC} = 5.0V