

74LCX16500

18-Bit Universal Bus Transceivers with 5V Tolerant Inputs and Outputs

General Description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output-enable OEAB is active-high. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and OEBA is active low).

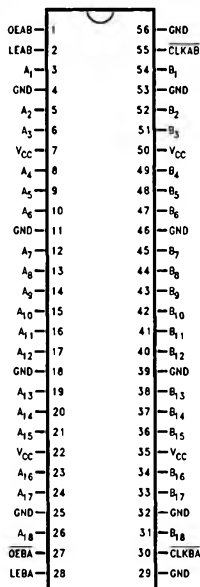
To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Features

- 6.0 ns t_{PD} max, 20 μ A I_{CCQ} max
- 5V tolerant inputs and outputs
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ± 24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 16500
- Latch-up performance exceeds 500 mA
- ESD performance:
 - Human body model > 2000V
 - Machine model > 200V

Connection Diagram

Pin Assignment for SSOP and TSSOP



Function Table†

Inputs				Output B
OEAB	LEAB	CLKAB	A	
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B ₀ ‡
H	L	L	X	B ₀ §

† A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

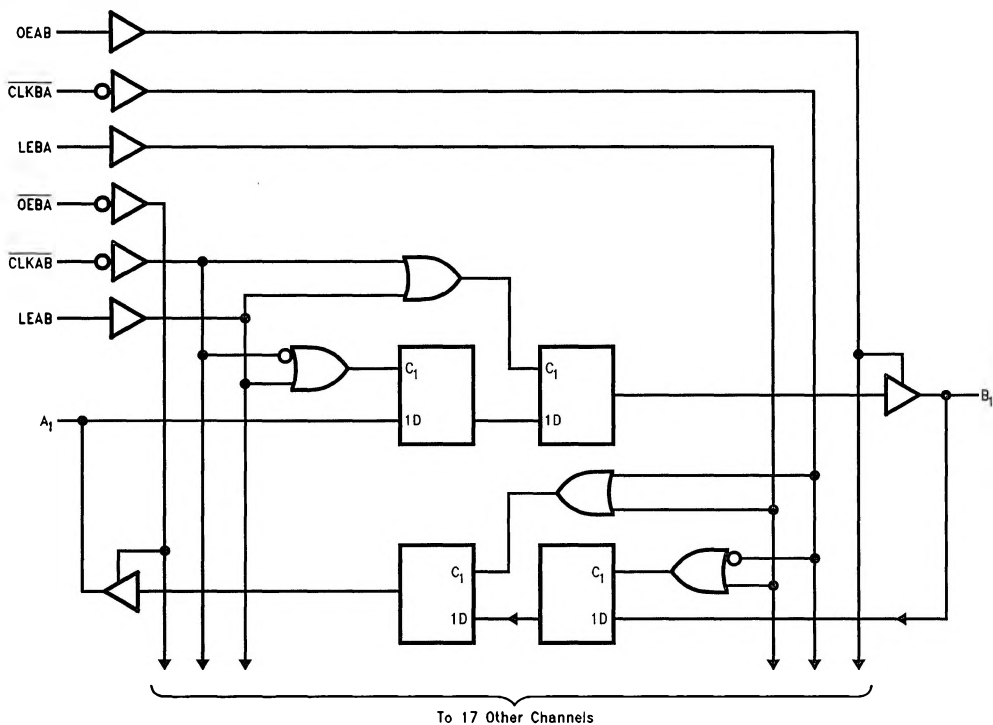
‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

TL/F/12407-1

Logic Diagram



TL/F/12407-2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	-0.5 to +7.0		V
V_I	DC Input Voltage	-0.5 to +7.0		V
V_O	DC Output Voltage	-0.5 to +7.0	Output in TRI-STATE®	V
		-0.5 to $V_{CC} + 0.5$	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	-50	$V_I < GND$	mA
I_{OK}	DC Output Diode Current	-50	$V_O < GND$	mA
		+50	$V_O > V_{CC}$	
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	-65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6
		Data Retention	1.5	3.6
V_I	Input Voltage	0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}
		TRI-STATE	0	5.5
I_{OH}/I_{OL}	Output Current	$V_{CC} = 3.0V - 3.6V$ $V_{CC} = 2.7V$	±24 ±12	mA
T_A	Free-Air Operating Temperature	-40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8V - 2.0V$, $V_{CC} = 3.0V$	0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40^{\circ}C$ to $+85^{\circ}C$		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7-3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7-3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.7-3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -12 mA$	2.7	2.2		V
		$I_{OH} = -18 mA$	3.0	2.4		V
		$I_{OH} = -24 mA$	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	2.7-3.6		0.2	V
		$I_{OL} = 12 mA$	2.7		0.4	V
		$I_{OL} = 16 mA$	3.0		0.4	V
		$I_{OL} = 24 mA$	3.0		0.55	V
I_I	Input Leakage Current	$0 \leq V_I \leq 5.5V$	2.7-3.6		±5.0	μA
I_{OZ}	TRI-STATE I/O Leakage	$0 \leq V_O \leq 5.5V$ $V_I = V_{IH}$ or V_{IL}	2.7-3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or $V_O = 5.5V$	0		100	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.7-3.6		20	μA
		$3.6V \leq V_I, V_O \leq 5.5V$	2.7-3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.7-3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	T _A = -40°C to +85°C				Units
		V _{CC} = 3.3V ±0.3V		V _{CC} = 2.7V		
		Min	Max (Note 1)	Min	Max (Note 1)	
f _{max}	Maximum Clock Frequency	170				MHz
t _{PHL} t _{PLH}	Propagation Delay Bus to Bus	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t _{PHL} t _{PLH}	Propagation Delay Clock to Bus	1.5 1.5	6.5 6.5	1.5 1.5	7.5 7.5	ns
t _{PHL} t _{PLH}	Propagation Delay LE to Bus	1.5 1.5	6.5 6.5	1.5 1.5	7.5 7.5	ns
t _{PZL} t _{PZH}	Output Enable Time	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns
t _{PLZ} t _{PHZ}	Output Disable Time	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t _s	Setup Time	2.5		2.5		ns
t _H	Hold Time	1.5		1.5		ns
t _W	Pulse Width	3.0		3.0		ns
t _{OSHL} t _{OSLH}	Output to Output Skew (Note 2)		1.0 1.0			ns

Note 1: The Maximum AC limits are design target. Actual performance will be specified upon completion of characterization.

Note 2: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C	Units
				Typical	
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V	3.3	0.8	V
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C _{IN}	Input Capacitance	V _{CC} = Open, V _I = 0V or V _{CC}	7	pF
C _{OUT}	Output Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC}	8	pF
C _{PD}	Power Dissipation Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC} , F = 10 MHz	20	pF

74LCX16500 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

