National Semiconductor

**ADVANCE INFORMATION**

# 74LVT16240
# 3.3V ABT 16-Bit Inverting Buffer/Line Driver with TRI-STATE® Outputs

## General Description

The LVT16240 contains sixteen inverting buffers with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/-receiver. The device is nibble controlled.

Individual TRI-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

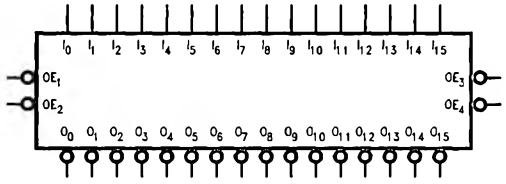
These buffers and line drivers are designed for low-voltage (3.3V) $V_{CC}$ applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16240 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

## Features

- Input and output interface capability to systems at 5V $V_{CC}$
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16240
- Latch-up performance exceeds 500 mA

## Ordering Code: See Section 11

## Logic Symbol



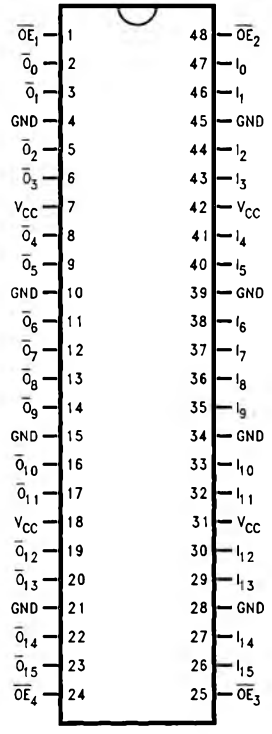

TL/F/12025–1

| Pin Names | Description |
|---|---|
| $\overline{OE}_n$ | Output Enable Inputs (Active Low) |
| $I_0$–$I_{15}$ | Inputs |
| $\overline{O}_0$–$\overline{O}_{15}$ | TRI-STATE Outputs |

| | SSOP | TSSOP JEDEC |
|---|---|---|
| Order Number | 74LVT16240MEA<br>74LVT16240MEAX | 74LVT16240MTD<br>74LVT16240MTDX |
| See NS Package Number | MS48A | MTD48 |

## Connection Diagram

**Pin Assignment for SSOP and TSSOP**

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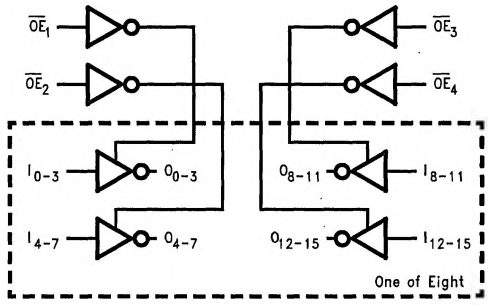
## Functional Description

The LVT16240 contains sixteen inverting buffers with TRI-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins may be shorted together to obtain full 16-bit operation. The TRI-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input for each nibble. When $\overline{OE}_n$ is LOW, the outputs are in 2-state mode. When $\overline{OE}_n$ is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

## Logic Diagram

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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Truth Tables

| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}_1$ | $I_0$–$I_3$ | $\overline{O}_0$–$\overline{O}_3$ |
| L | L | H |
| L | H | L |
| H | X | Z |

| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}_2$ | $I_4$–$I_7$ | $\overline{O}_4$–$\overline{O}_7$ |
| L | L | H |
| L | H | L |
| H | X | Z |

| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}_3$ | $I_8$–$I_{11}$ | $\overline{O}_8$–$\overline{O}_{11}$ |
| L | L | H |
| L | H | L |
| H | X | Z |

| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}_4$ | $I_{12}$–$I_{15}$ | $\overline{O}_{12}$–$\overline{O}_{15}$ |
| L | L | H |
| L | H | L |
| H | X | Z |

H = High Voltage Level  L = Low Voltage Level

X = Immaterial  Z = High Impedance