National Semiconductor

ADVANCE INFORMATION

74LVT16245
3.3V ABT 16-Bit Transceiver with TRI-STATE® Outputs

General Description

The LVT16245 contains sixteen non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus oriented applications. The device is byte controlled. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The $T/\overline{R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B ports by placing them in a high impedance state.

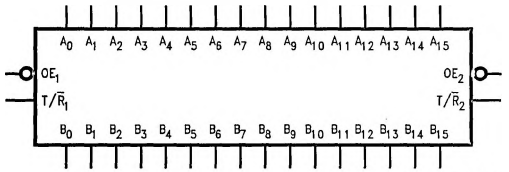
This non-inverting transceiver is designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16245 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16245
- Latch-up performance exceeds 500 mA

Ordering Code: See Section 11

Logic Symbol



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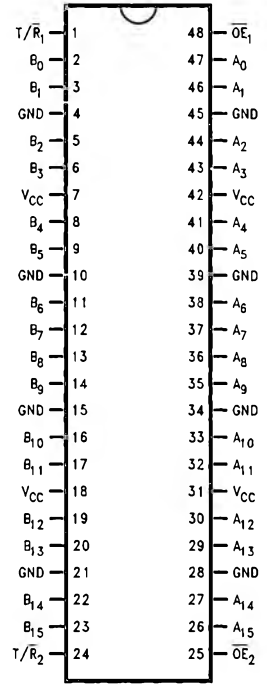
Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
$T/\overline{R}_n$	Transmit/Receive Input
A_0–A_{15}	Side A Inputs/TRI-STATE Outputs
B_0–B_{15}	Side B Inputs/TRI-STATE Outputs

	SSOP	TSSOP JEDEC
Order Number	74LVT16245MEA 74LVT16245MEAX	74LVT16245MTD 74LVT16245MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP



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Functional Description

The LVT16245 contains sixteen non-inverting bidirectional buffers with TRI-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

Truth Tables

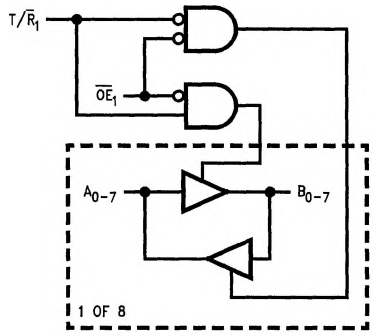
Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH-Z State on A_0–A_7, B_0–B_7

H = High Voltage Level L = Low Voltage Level

Inputs		Outputs
$\overline{OE}_2$	$T/\overline{R}_2$	
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH-Z State on A_8–A_{15}, B_8–B_{15}

X = Immaterial Z = High Impedance

Logic Diagrams



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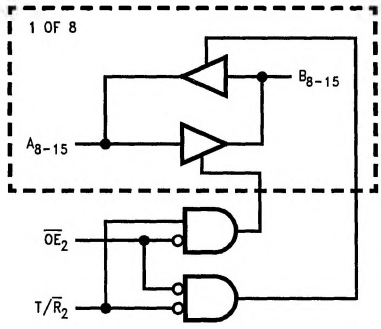

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Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.