National Semiconductor

ADVANCE INFORMATION

74LVT374
3.3V ABT Octal D Flip-Flop with TRI-STATE® Outputs

General Description

The LVT374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

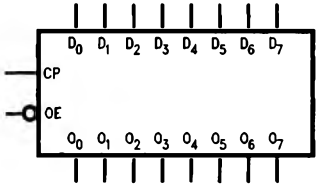
These octal flip-flops are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT374 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP
- Functionally compatible with the 74 series 374
- Latch-up performance exceeds 500 mA

Ordering Code: See Section 11

Logic Symbols



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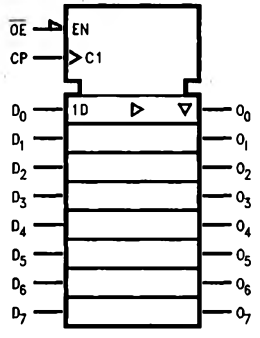
IEEE/IEC



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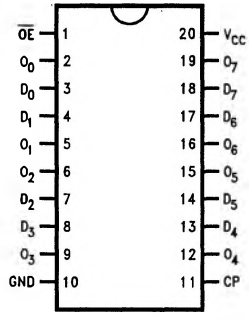
Connection Diagram

Pin Assignment for SOIC and TSSOP



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Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP JEDEC
Order Number	74LVT374WM 74LVT374WMX	74LVT374SJ 74LVT374SJX	74LVT374MTCX
See NS Package Number	M20B	M20D	MTC20

Functional Description

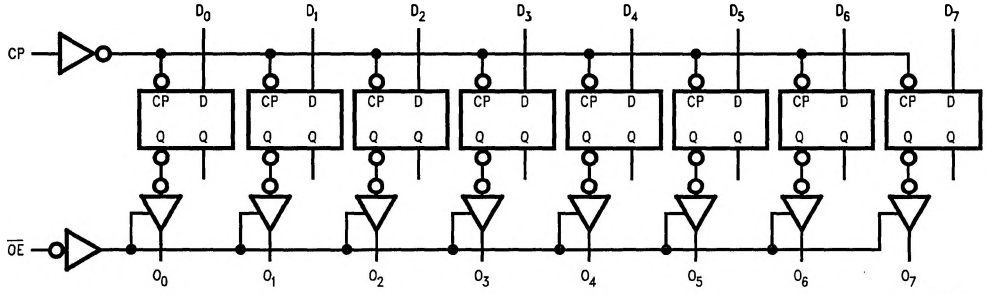
The LVT374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	⌐‾	L	H
L	⌐‾	L	L
X	L	L	O_o
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐‾ = LOW-to-HIGH Transition
O_o = Previous O_o before HIGH to LOW of CP

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.