National Semiconductor

74LVX273
Low Voltage Octal D Flip-Flop

General Description

The LVX273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

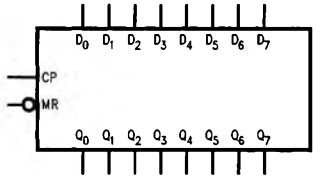
All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

Features

- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Ordering Code: See Section 11

Logic Symbols



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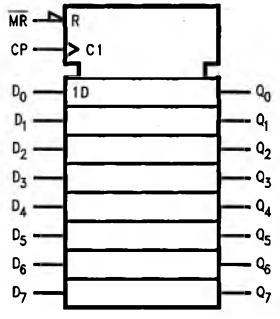
IEEE/IEC



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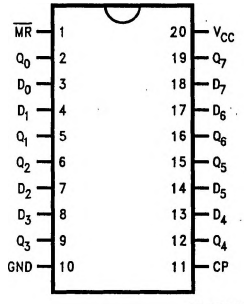
Connection Diagram

Pin Assignment for SOIC and SSOP



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Pin Names	Description
D_0–D_7	Data Inputs
$\overline{MR}$	Master Reset
CP	Clock Pulse Input
Q_0–Q_7	Data Outputs

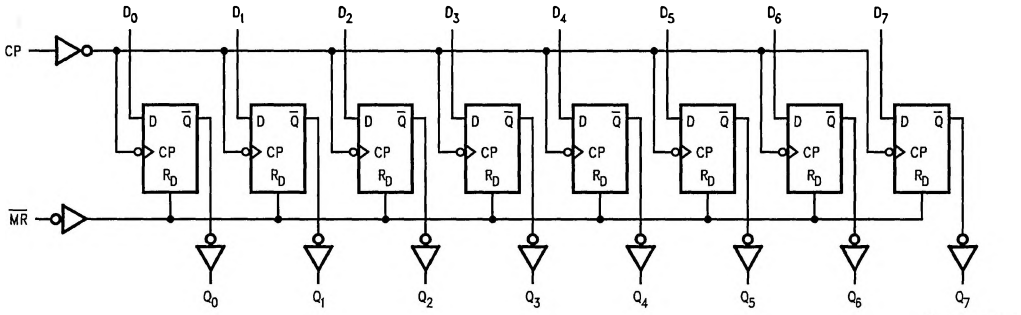
	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX273M 74LVX273MX	74LVX273SJ 74LVX273SJX	74LVX273MSCX
See NS Package Number	M20B	M20D	MSC20

Mode Select-Function Table

Operating Mode	Inputs			Outputs
	$\overline{MR}$	CP	D_n	Q_n
Reset (Clear)	L	X	X	L
Load '1'	H	⌐	H	H
Load '0'	H	⌐	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation	180 mW

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time ($\Delta t/\Delta V$)	0 ns/V to 100 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	74LVX273 T_A = +25°C			74LVX273 T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V		
V_{IL}	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V		
V_{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA I_{OH} = −50 μA I_{OH} = −4 mA
V_{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 4 mA
I_{OZ}	TRI-STATE® Output Off-State Current	3.6			±0.25		±2.5	μA	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND	
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			4.0		40.0	μA	V_{IN} = V_{CC} or GND	

Noise Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX273 T_A = 25°C		Units	C_L (pF)
			Typ	Limit		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.5	0.8	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.5	−0.8	V	50
V_{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: Input t_r = t_f = 3 ns

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX273 $T_A = +25°C$ Min	Typ	Max	74LVX273 $T_A = -40°C$ to $+85°C$ Min	Max	Units	C_L (pF)
t_{PLH} t_{PHL}	Propagation Delay Time CP to Q_n	2.7		9.0	16.9	1.0	20.5	ns	15
				11.5	20.4	1.0	24.0		50
		3.3 ±0.3		7.1	11.0	1.0	13.0		15
				9.6	14.5	1.0	16.5		50
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	2.7		9.3	17.8	1.0	20.5	ns	15
				11.8	21.1	1.0	24.0		50
		3.3 ±0.3		7.3	11.5	1.0	13.5		15
				9.8	15.0	1.0	17.0		50
t_S	Setup Time D_n to CP	2.7	8.0			9.5		ns	
		3.3 ±0.3	5.5			6.5			
t_H	Hold Time D_n to CP	2.7	1.0			1.0		ns	
		3.3 ±0.3	1.0			1.0			
t_{REM}	Removal Time $\overline{MR}$ to CP	2.7	4.0			4.0		ns	
		3.3 ±0.3	2.5			2.5			
t_W	Clock Pulse Width	2.7	8.0			9.5		ns	
		3.3 ±0.3	5.5			6.5			
t_W	$\overline{MR}$ Pulse Width	2.7	7.5			8.5		ns	
		3.3 ±0.3	5.0			6.0			
f_{MAX}	Maximum Clock Frequency	2.7	55	110		45		MHz	15
			45	60		40			50
		3.3 ±0.3	95	150		80			15
			60	90		50			50
t_{OSLH} t_{OSHL}	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	50

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Capacitance

Symbol	Parameter	74LVX273 $T_A = +25°C$ Min	Typ	Max	74LVX273 $T_A = -40°C$ to $+85°C$ Min	Max	Units
C_{IN}	Input Capacitance		4	10		10	pF
C_{OUT}	Output Capacitance		6				pF
C_{PD}	Power Dissipation Capacitance (Note 1)		31				pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{8 \text{ (per F/F)}}$