National Semiconductor

# 74LVX3245
# 8-Bit Dual Supply Translating Transceiver with TRI-STATE® Outputs

## General Description

The LVX3245 is a dual-supply, 8-bit translating transceiver that is designed to interface between a 3V bus and a 5V bus in a mixed 3V/5V supply environment. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition. The A port interfaces with the 3V bus; the B port interfaces with the 5V bus.

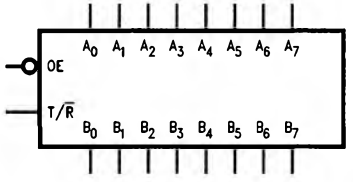
The LVX3245 is suitable for mixed voltage applications such as notebook computers using 3.3V CPU and 5V peripheral components.

## Features

- Bidirectional interface between 3V and 5V buses
- Inputs compatible with TTL level
- 3V data flow at A port and 5V data flow at B port
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Available in SOIC and QSOP packages
- Implements proprietary EMI reduction circuitry
- Functionally compatible with the 74 series 245

## Ordering Code: See Section 11

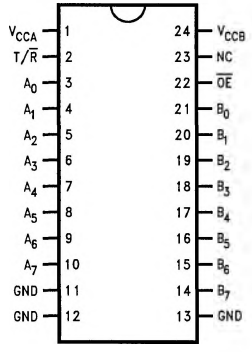
## Logic Symbol




TL/F/11620–1

## Connection Diagram

**Pin Assignment for SOIC and QSOP**




TL/F/11620–2

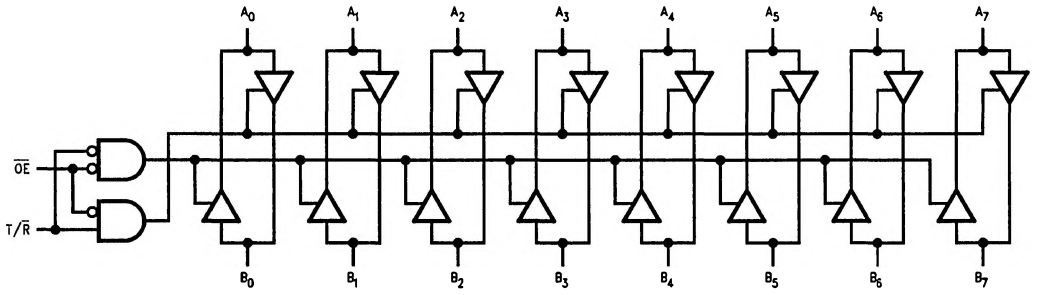
| Pin Names | Description |
|---|---|
| $\overline{OE}$ | Output Enable Input |
| $T/\overline{R}$ | Transmit/Receive Input |
| $A_0$–$A_7$ | Side A Inputs or TRI-STATE Outputs |
| $B_0$–$B_7$ | Side B Inputs or TRI-STATE Outputs |

| | SOIC JEDEC | QSOP |
|---|---|---|
| Order Number | 74LVX3245WM<br>74LVX3245WMX | 74LVX3245QSC<br>74LVX3245QSCX |
| See NS Package Number | M24B | MQA24 |

## Truth Table

| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}$ | T/$\overline{R}$ | |
| L | L | Bus B Data to Bus A |
| L | H | Bus A Data to Bus B |
| H | X | HIGH-Z State |

## Logic Diagram

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## Absolute Maximum Ratings (Note)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CCA}$, $V_{CCB}$) | −0.5V to +7.0V |
| DC Input Voltage ($V_I$) @ $\overline{OE}$, T/$\overline{R}$ | −0.5V to $V_{CCB}$ + 0.5V |
| DC Input/Output Voltage ($V_{I/O}$) | |
| @ A(n) | −0.5V to $V_{CCA}$ + 0.5V |
| @ B(n) | −0.5V to $V_{CCB}$ + 0.5V |
| DC Input Diode Current ($I_{IN}$) @ $\overline{OE}$, T/$\overline{R}$ | ±20 mA |
| DC Output Diode Current ($I_{OK}$) | ±50 mA |
| DC Output Source or Sink Current ($I_O$) | ±50 mA |
| DC $V_{CC}$ or Ground Current per Output Pin ($I_{CC}$ or $I_{GND}$) | ±50 mA |
| and Max Current @ $I_{CCA}$ | ±100 mA |
| @ $I_{CCB}$ | ±200 mA |
| Storage Temperature Range ($T_{STG}$) | −65°C to +150°C |
| DC Latch-Up Source or Sink Current | ±300 mA |

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage | |
| $V_{CCA}$ | 2.7V to 3.6V |
| $V_{CCB}$ | 4.5V to 5.5V |
| Input Voltage ($V_I$) @ $\overline{OE}$, T/$\overline{R}$ | 0V to $V_{CCB}$ |
| Input/Output Voltage ($V_{I/O}$) | |
| @ A(n) | 0V to $V_{CCA}$ |
| @ B(n) | 0V to $V_{CCB}$ |
| Free Air Operating Temperature ($T_A$) | |
| 74LVX | −40°C to +85°C |
| Minimum Input Edge Rate ($\Delta t/\Delta V$) | 8 ns/V |
| $V_{IN}$ from 30% to 70% of $V_{CC}$ | |
| $V_{CC}$ @ 3.0V, 4.5V, 5.5V | |

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

## DC Electrical Characteristics

| Symbol | Parameter | | $V_{CCA}$ (V) | $V_{CCB}$ (V) | 74LVX3245 $T_A$ = +25°C | 74LVX3245 $T_A$ = −40°C to +85°C | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Typ | Guaranteed Limits | | | |
| $V_{IHA}$ | Minimum High Level Input Voltage | A(n), T/$\overline{R}$, $\overline{OE}$ | 3.6 | 5.0 | | 2.0 | 2.0 | V | $V_{OUT} \leq$ 0.1V or $\geq V_{CC}$ − 0.1V |
| | | | 2.7 | 5.0 | | 2.0 | 2.0 | | |
| $V_{IHB}$ | | B(n) | 3.3 | 4.5 | | 2.0 | 2.0 | | |
| | | | 3.3 | 5.5 | | 2.0 | 2.0 | | |
| $V_{ILA}$ | Maximum Low Level Input Voltage | A(n), T/$\overline{R}$, $\overline{OE}$ | 3.6 | 5.0 | | 0.8 | 0.8 | V | $V_{OUT} \leq$ 0.1V or $\geq V_{CC}$ −0.1V |
| | | | 2.7 | 5.0 | | 0.8 | 0.8 | | |
| $V_{ILB}$ | | B(n) | 3.3 | 4.5 | | 0.8 | 0.8 | | |
| | | | 3.3 | 5.5 | | 0.8 | 0.8 | | |
| $V_{OHA}$ | Minimum High Level Output Voltage | | 3.0 | 4.5 | 2.99 | 2.9 | 2.9 | V | $I_{OUT}$ = −100 μA |
| | | | 3.0 | 4.5 | 2.65 | 2.35 | 2.25 | | $I_{OH}$ = −24 mA |
| | | | 2.7 | 4.5 | 2.5 | 2.3 | 2.2 | | $I_{OH}$ = −12 mA |
| | | | 2.7 | 4.5 | 2.3 | 2.1 | 2.0 | | $I_{OH}$ = −24 mA |
| $V_{OHB}$ | | | 3.0 | 4.5 | 4.5 | 4.4 | 4.4 | V | $I_{OUT}$ = −100 μA |
| | | | 3.0 | 4.5 | 4.25 | 3.86 | 3.76 | | $I_{OH}$ = −24 mA |
| $V_{OLA}$ | Maximum Low Level Output Voltage | | 3.0 | 4.5 | 0.002 | 0.1 | 0.1 | V | $I_{OUT}$ = 100 μA |
| | | | 3.0 | 4.5 | 0.21 | 0.36 | 0.44 | | $I_{OL}$ = 24 mA |
| | | | 2.7 | 4.5 | 0.11 | 0.36 | 0.44 | | $I_{OL}$ = 12 mA |
| | | | 2.7 | 4.5 | 0.22 | 0.42 | 0.5 | | $I_{OL}$ = 24 mA |
| $V_{OLB}$ | | | 3.0 | 4.5 | 0.002 | 0.1 | 0.1 | V | $I_{OUT}$ = 100 μA |
| | | | 3.0 | 4.5 | 0.18 | 0.36 | 0.44 | | $I_{OL}$ = 24 mA |
| $I_{IN}$ | Maximum Input Leakage Current @ $\overline{OE}$, T/$\overline{R}$ | | 3.6 | 5.5 | | ±0.1 | ±1.0 | μA | $V_I = V_{CCB}$, GND |
| $I_{OZA}$ | Maximum TRI-STATE Output Leakage @ A(n) | | 3.6 | 5.5 | | ±0.5 | ±5.0 | μA | $V_I = V_{IL}, V_{IH}$ $\overline{OE} = V_{CCA}$ $V_O = V_{CCA}$, GND |

## DC Electrical Characteristics (Continued)

| Symbol | Parameter | | $V_{CCA}$ (V) | $V_{CCB}$ (V) | 74LVX3245 $T_A = +25°C$ | 74LVX3245 $T_A = -40°C$ to $+85°C$ | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Typ | Guaranteed Limits | | | |
| $I_{OZB}$ | Maximum TRI-STATE Output Leakage @ B(n) | | 3.6 | 5.5 | | ±0.5 | ±5.0 | μA | $V_I = V_{IL}, V_{IH}$<br>$\overline{OE} = V_{CCA}$<br>$V_O = V_{CCB}$, GND |
| $\Delta I_{CC}$ | Maximum $I_{CCT}$/Input @ | B(n) | 3.6 | 5.5 | 1.0 | 1.35 | 1.5 | mA | $V_I = V_{CCB} - 2.1V$ |
| | | A(n), T/$\overline{R}$, $\overline{OE}$ | 3.6 | 5.5 | | 0.35 | 0.5 | mA | $V_I = V_{CCA} - 0.6V$ |
| $I_{CCA}$ | Quiescent $V_{CCA}$ Supply Current | | 3.6 | 5.5 | | 5 | 50 | μA | A(n) = $V_{CCA}$ or GND<br>B(n) = $V_{CCB}$ or GND,<br>$\overline{OE}$ = GND, T/$\overline{R}$ = GND |
| $I_{CCB}$ | Quiescent $V_{CCB}$ Supply Current | | 3.6 | 5.5 | | 8 | 80 | μA | A(n) = $V_{CCA}$ or GND<br>B(n) = $V_{CCB}$ or GND,<br>$\overline{OE}$ = GND, T/$\overline{R}$ = $V_{CCA}$ |
| $V_{OLPA}$<br>$V_{OLPB}$ | Quiet Output Maximum Dynamic $V_{OL}$ | | 3.3<br>3.3 | 5.0<br>5.0 | | 0.8<br>1.5 | | V | (Notes 1, 2) |
| $V_{OLVA}$<br>$V_{OLVB}$ | Quiet Output Minimum Dynamic $V_{OL}$ | | 3.3<br>3.3 | 5.0<br>5.0 | | −0.8<br>−1.2 | | V | (Notes 1, 2) |
| $V_{IHDA}$<br>$V_{IHDB}$ | Minimum High Level Dynamic Input Voltage | | 3.3<br>3.3 | 5.0<br>5.0 | | 2.0<br>2.0 | | V | (Notes 1, 3) |
| $V_{ILDA}$<br>$V_{ILDB}$ | Maximum Low Level Dynamic Input Voltage | | 3.3<br>3.3 | 5.0<br>5.0 | | 0.8<br>0.8 | | V | (Notes 1, 3) |

†Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** Worst case package.

**Note 2:** Max number of outputs defined as (n). Data inputs are driven 0V to $V_{CC}$ level; one output at GND.

**Note 3:** Max number of Data Inputs (n) switching. (n−1) inputs switching 0V to $V_{CC}$ level. Input-under-test switching: $V_{CC}$ level to threshold ($V_{IHD}$), 0V to threshold ($V_{ILD}$), f = 1 MHz.

## AC Electrical Characteristics: See Section 2 for Test Methodology

| Symbol | Parameters | 74LVX3245 $T_A = +25°C$, $C_L = 50$ pF, **$V_{CCA} = 3.3V$, *$V_{CCB} = 5.0V$ | | | 74LVX3245 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, **$V_{CCA} = 3.3V$, *$V_{CCB} = 5.0V$ | | 74LVX3245 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $V_{CCA} = 2.7V$, *$V_{CCB} = 5.0V$ | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Max | Min | Max | |
| $t_{PHL}$<br>$t_{PLH}$ | Propagation Delay<br>A to B | 1.0<br>1.0 | 5.4<br>5.6 | 8.0<br>7.5 | 1.0<br>1.0 | 8.5<br>8.0 | 1.0<br>1.0 | 9.0<br>8.5 | ns |
| $t_{PHL}$<br>$t_{PLH}$ | Propagation Delay<br>B to A | 1.0<br>1.0 | 5.1<br>5.7 | 7.5<br>7.5 | 1.0<br>1.0 | 8.0<br>8.0 | 1.0<br>1.0 | 8.5<br>8.5 | ns |
| $t_{PZL}$<br>$t_{PZH}$ | Output Enable<br>Time $\overline{OE}$ to B | 1.0<br>1.0 | 4.8<br>6.3 | 8.0<br>8.5 | 1.0<br>1.0 | 8.5<br>9.0 | 1.0<br>1.0 | 9.0<br>9.5 | ns |
| $t_{PZL}$<br>$t_{PZH}$ | Output Enable<br>Time $\overline{OE}$ to A | 1.0<br>1.0 | 6.3<br>6.8 | 8.5<br>9.0 | 1.0<br>1.0 | 9.0<br>9.5 | 1.0<br>1.0 | 9.5<br>10.0 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable<br>Time $\overline{OE}$ to B | 1.0<br>1.0 | 5.3<br>4.2 | 7.5<br>7.0 | 1.0<br>1.0 | 8.0<br>7.5 | 1.0<br>1.0 | 8.5<br>8.0 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable<br>Time $\overline{OE}$ to A | 1.0<br>1.0 | 5.3<br>3.7 | 8.0<br>6.5 | 1.0<br>1.0 | 8.5<br>7.0 | 1.0<br>1.0 | 9.0<br>7.5 | ns |
| $t_{OSHL}$<br>$t_{OSLH}$ | Output to Output Skew***<br>Data to Output | | 1.0 | 1.5 | | 1.5 | | 1.5 | ns |

*Voltage Range 5.0V is 5.0V ±0.5V.
**Voltage Range 3.3V is 3.3V ±0.3V.

***Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW ($t_{OSHL}$) or LOW to HIGH ($t_{OSLH}$). Parameter guaranteed by design.

## Capacitance

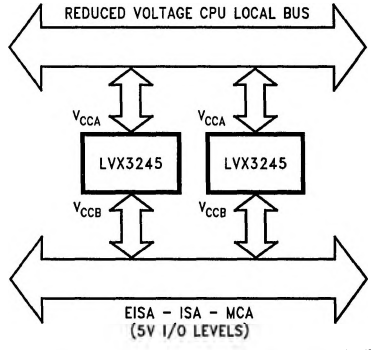
| Symbol | Parameter | | Typ | Units | Conditions |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | 4.5 | pF | $V_{CC}$ = Open |
| $C_{I/O}$ | Input/Output Capacitance | | 15 | pF | $V_{CCA} = 3.3V$<br>$V_{CCB} = 5.0V$ |
| $C_{PD}$ | Power Dissipation Capacitance | A → B | 55 | pF | $V_{CCB} = 5.0V$ |
| | | B → A | 40 | | $V_{CCA} = 3.3V$ |

$C_{PD}$ is measured at 10 MHz

## 8-Bit Dual Supply Translating Transceiver

The LVX3245 is a dual supply device capable of bidirectional signal translation. This level shifting ability provides an efficient interface between low voltage CPU local bus with memory and a standard bus defined by 5V I/O levels. The device control inputs can be controlled by either the low voltage CPU and core logic or a bus arbitrator with 5V I/O levels.

Manufactured on a sub-micron CMOS process, the LVX3245 is ideal for mixed voltage applications such as notebook computers using 3.3V CPU's and 5V peripheral devices.




TL/F/11620–3