**National Semiconductor**

# 74LVX3L384
# 10-Bit Low Power Bus Switch

## General Description

The LVX3L384 provides 10 bits of high-speed CMOS TTL-compatible bus switches. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. The device is organized as two 5-bit switches with separate bus enable ($\overline{BE}$) signals. When $\overline{BE}$ is low, the switch is on and port A is connected to port B. When $\overline{BE}$ is high, the switch is open and a high-impedance state exists between the two ports.

## Features

- 5Ω switch connection between two ports
- Zero propagation delay
- Ultra low power with 0.2 $\mu$A typical $I_{CC}$
- Zero ground bounce in flow-through mode
- Control inputs compatible with TTL level
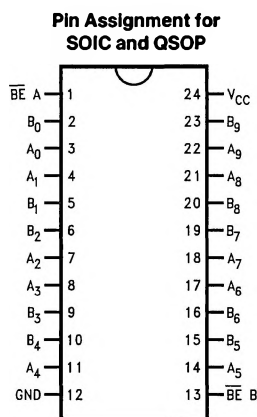- Available in SOIC and QSOP (SSOP 0.15″ Body width)

## Ordering Code: See Section 11

## Logic Diagram
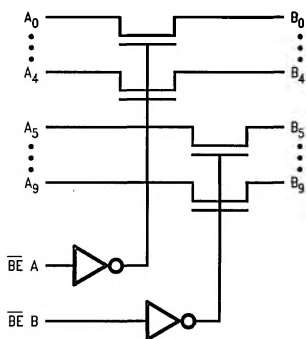


TL/F/11653–1

## Connection Diagram

**Pin Assignment for SOIC and QSOP**



TL/F/11653–2

## Truth Table

| $\overline{BE}$ A | $\overline{BE}$ B | $B_0$–$B_4$ | $B_5$–$B_9$ | Function |
|---|---|---|---|---|
| L | L | $A_0$–$A_4$ | $A_5$–$A_9$ | Connect |
| L | H | $A_0$–$A_4$ | HIGH-Z State | Connect |
| H | L | HIGH-Z State | $A_5$–$A_9$ | Connect |
| H | H | HIGH-Z State | HIGH-Z State | Disconnect |

| Pin Names | Description |
|---|---|
| $\overline{BE}$ A, $\overline{BE}$ B | Bus Switch Enable |
| $A_0$–$A_9$ | Bus A |
| $B_0$–$B_9$ | Bus B |

| | SOIC JEDEC | SSOP JEDEC |
|---|---|---|
| Order Number | 74LVX3L384WM<br>74LVX3L384WMX | 74LVX3L384QSC<br>74LVX3L384QSCX |
| See NS Package Number | M24B | MQA24 |

**Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.**

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | $-0.5V$ to $+7.0V$ |
| DC Switch Voltage ($V_S$) | $-0.5$ to $+7.0V$ |
| DC Input Input Voltage ($V_I$) (Note 2) | $-0.5$ to $+7.0V$ |
| DC Input Diode Current with ($V_I < 0$) | $-20$ mA |
| DC Output ($I_O$) Sink Current | 120 mA |
| Storage Temperature Range ($T_{STG}$) | $-65°C$ to $+150°C$ |
| Power Dissipation | 0.5W |

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 2: *The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.*

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | 4.0V to 5.5V |
| Free Air Operating Temperature ($T_A$) | $-40°C$ to $+85°C$ |

## DC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) | 74LVX3L384 $T_A = -40°C$ to $+85°C$ Min | Typ (Note 3) | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Maximum Clamp Diode Voltage | 4.5 | | | $-1.2$ | V | $I_{IN} = -18$ mA |
| $V_{IH}$ | Minimum High Level Input Voltage | 4.0–5.5 | 2.0 | | | V | |
| $V_{IL}$ | Maximum Low Level Input Voltage | 4.0–5.5 | | | 0.8 | | |
| $I_{IN}$ | Maximum Input Leakage Current | 0 | | | 10 | $\mu$A | $0 \le V_{IN} \le 5.5V$ |
| | | 5.5 | | | $\pm 1$ | | |
| $I_{OZ}$ | Maximum TRI-STATE® I/O Leakage | 5.5 | | | $\pm 1$ | $\mu$A | $0 \le A, B \le V_{CC}$ |
| $I_{OS}$ | Short Circuit Current | 4.5 | 100 | | | mA | $V_I(A), V_I(B) = 0V,$ $V_I(B), V_I(A) = 4.5V$ |
| $R_{ON}$ | Switch On Resistance (Note 1) | 4.5 | | 5 | 7 | $\Omega$ | $V_I = 0V, I_{ON} = 30$ mA |
| | | | | 10 | 15 | $\Omega$ | $V_I = 2.4V, I_{ON} = 15$ mA |
| $I_{CC}$ | Maximum Quiescent Supply Current | 5.5 | | 0.2 | 3.0 | $\mu$A | $V_I = V_{CC}, GND$ $I_O = 0$ |
| $\Delta I_{CC}$ | Increase in $I_{CC}$ per Input (Note 2) | 5.5 | | | 2.5 | mA | $V_{IN} = 3.4V, I_O = 0$ Per Control Input |

**Note 1:** Measured by voltage drop between A and B pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

**Note 2:** Per TTL driven input ($V_{IN} = 3.4V$, control inputs only). A and B pins do not contribute to $I_{CC}$.

**Note 3:** All typical values are at $V_{CC} = 5.0V$, $T_A = 25°C$.

## AC Electrical Characteristics: See Section 2 for Test Methodology

| Symbol | Parameter | V_CC (V) | 74LVX3L384 T_A = −40°C to +85°C C_L = 50 pF | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ (Note 2) | Max | |
| $T_{PLH}$ $T_{PHL}$ | Data Propagation Delay An to Bn or Bn to An (Note 1) | 4.5 | | | 0.25 | ns |
| $T_{PZL}$ $T_{PZH}$ | Switch Enable Time $\overline{BE}_A$, $\overline{BE}_B$ to An, Bn | 4.5 | 1.5 | | 6.5 | ns |
| $T_{PLZ}$ $T_{PHZ}$ | Switch Disable Time $\overline{BE}_A$, $\overline{BE}_B$ to An, Bn | 4.5 | 1.5 | | 5.5 | ns |

**Note 1:** This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On resistance of the switch and the load capacitance. The time constant for the switch and alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

**Note 2:** All typical values are at $V_{CC}$ = 5.0V, $T_A$ = 25°C.

## Capacitance (Note)

| Symbol | Parameter | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|
| $C_{IN}$ | Control Input Capacitance | 4 | | pF | $V_{CC}$ = 5.0V |
| $C_{I/O}$ (ON) | Input/Output Capacitance | 8 | | pF | $V_{CC}$ = 5.0V |
| $C_{I/O}$ (OFF) | Input/Output Capacitance | 6 | | pF | $V_{CC}$ = 5.0V |

**Note:** Capacitance is characterized but not tested.