signetics

2048 BIT BIPOLAR ROM (256x8 ROM)
4096 BIT BIPOLAR ROM (512x8 ROM)

8204
8205

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 8205 and 8204 are high performance bipolar ROM's incorporating the storage output or memory data register into the chip. Data is addressed by applying address information to the address lines. After valid data appears at the output of the memory array, (typically 35ns after the address is applied) and if the circuit is enabled, the strobe pulse will enter data into the 8 bit output latch register. A D-type latch (L) is used to enable the tri-state output drivers. If the circuit enable signals are valid, the strobe will set the latch. This turns on the output stage. The latch will remain set and keep the output enabled until the chip is disabled and the next strobe pulse occurs. If the strobe line is held high, the ROM will function in a conventional mode. The output will be controlled solely by the chip enable and the output latches will be bypassed.

See page 4-34 for ASCII (ADDRESS) to EBCDIC (DATA) and EBCDIC (ADDRESS) to ASCII (DATA) and 4-35/ for 4-53 for ORDERING BLANKS.

APPLICATIONS

- MICROPROGRAMMING
- HARDWIRE ALGORITHMS
- CHARACTER GENERATION
- CONTROL STORE

FEATURES

BUFFERED ADDRESS LINES

ON THE CHIP DECODING

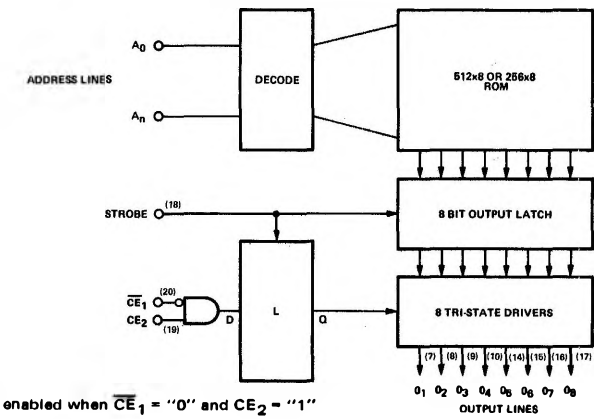
ON THE CHIP STORAGE LATCHES

TRI-STATE OUTPUT

PROTECTED INPUTS

BLOCK DIAGRAM

8204 (256x8) AND 8205 (512x8) MEMORY ORGANIZATION



Chip is enabled when $\overline{CE}_1$ = "0" and CE_2 = "1"

Address Pins	8204	8205
A_0	(21)	(20)
A_1	(22)	(21)
A_2	(23)	(23)
A_3	(1)	(1)
A_4	(2)	(2)
A_5	(4)	(3)
A_6	(5)	(4)
A_7	(6)	(5)
A_8	–	(6)

V_{CC} = (24)
GND = (12)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 75°C$; $4.75V \leq V_{CC} \leq 5.25V$)

CHARACTERISTICS	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	NOTES
Input "0" Current			-100	μA	V_{in} = 0.5V	
Input "1" Current			25	μA	V_{in} = 5.25V	
Input (0) Threshold Voltage			.85	V		
Input (1) Threshold Voltage	2			V		
Input Clamp Voltage	-1.0			V	I_{in} = -5.0mA	
Output (0) Current		0.2	0.5	V	I_{out} = 9.6 mA	
Output (1) Current	2.7	3.3		V	I_{out} = -2.0mA	
Output (1) Short Circuit Current	-20	-35	-70	mA	V_{out} = 0V, V_{CC} = 5.0V	2
Input Capacitance		5		pF	V_{IH} = 2.0V, V_{CC} = 5.0V	
Output Capacitance		8		pF	V_{out} = 2.0V; V_{CC} = 5.0V	5
Power Supply Current		135	170	mA	V_{CC} = 5.0V	
Output (1) off Leakage Current (Chip Disabled)			100	μA	V_{in} = 2.7V	
Output (0) off Leakage Current (Chip Disabled)			-100	μA	V_{in} = 0.5V	

T_A = 25°C and V_{CC} = 5.0V

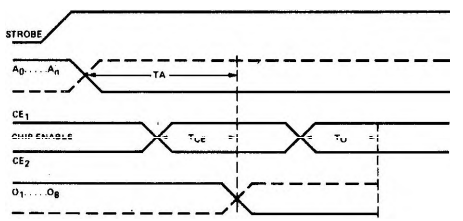
CHARACTERISTICS	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	NOTES
Address Access Time T_A		35	60	ns	Read Mode I or Read Mode II	6
Address Hold Time T_{ADS}	0	-10		ns	Read Mode 2 Only	6
Chip Enable Access Time T_{CE}		20	45	ns	Read Mode I or Read Mode II	6
Chip Enable Hold Time T_{CDS}	12	5		ns	Read Mode II Only	6
Output Disable Time T_O		20	45	ns	Read Mode I or Read Mode II	6
Strobe Pulse Width T_{SW}	33	20		ns	Read Mode II Only	6
Strobe Set-Up Time T_S		30	60	ns	Read Mode II Only	6
Output Disable Time T_R		18	32	ns	Read Mode I Only	6

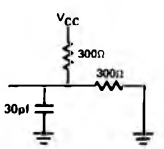
NOTES:

1. Positive current is defined as into the terminal referenced.
2. No more than one output should be grounded at the same time and strobe should be disabled. Strobe is in "1" state.
3. Manufacturer reserves the right to make design and process changes and improvements.
4. Applied voltages must not exceed 5.5V.
   Input currents must not exceed ±30 mA.
   Output currents must not exceed ±100 mA.
   Storage temperature must be between -60°C to +150°C.
5. Chip disabled.
6. Rise and fall times for tests must be less than 5ns. Input amplitudes are 2.8V and all measurements are made at 1.5V.

MEMORY TIMING

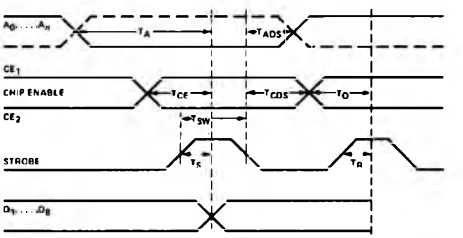
READ MODE I (OUTPUT LATCHES NOT USED)



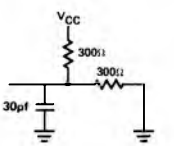


If the strobe is high, the device functions in a manner identical to conventional bipolar ROM's. The timing diagram shows valid data will appear T_A nanoseconds after the address has changed and T_{CE} nanoseconds after the output circuit is enabled. T_O is the time required to disable the output and switch it to an 'off' or high impedance state after it has been enabled.

READ MODE II (OUTPUT LATCHES USED)



NOTE: Outputs are undefined during the strobe setup time, T_S



In Read Mode II, the address is applied to the memory element T_A ns before output details desired. Applying the chip enable does not directly enable the outputs. When the strobe is applied T_S nanoseconds before the output, data from the memory array is copied into the output latches and the chip enable signal is copied into the delay latch L. The latch L in turn enables the output. After the strobe reaches the strobe level, both the chip enable and address lines may be altered but the output data stored in the latches will remain unchanged and the output of the circuit will remain enabled. The output will stay enabled until another strobe copies a Not chip enable signal into the latch L. The switching of the output to the "off" or high impedance state occurs T_R nanoseconds after the strobe.