2-INPUT 4-BIT DIGITAL MULTIPLEXER

8233 8234 8235

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

These devices are 2-input, 4-Bit Digital Multiplexers designed for general purpose data-selection applications.

The 8233 features *non-inverting* data paths; and, the 8234 features *inverting* data paths.

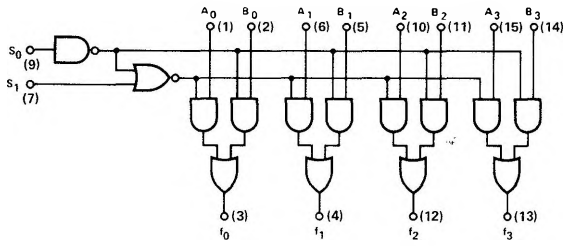
The 8235 is designed for input to adders, registers and general paralleled data handling due to its capability to perform CONDITIONAL COMPLEMENTING (TRUE/COMPLEMENT). When the two inputs for each bit position (Ai, Bi) are connected together, the f output will provide either the *True* or *Complement* of the input data. This capability is especially useful for transferring data into parallel adders where both true data for adding or multiplying and also complemented data for subtracting or dividing are needed.

The 8234 and 8235 designs have open collector outputs which permit direct wiring to other open collector outputs (collector logic) to yield "free" four-bit words. As many as one hundred four-bit words can be multiplexed by using fifty 8234/8235s in the WIRED-AND mode.

The inhibit state $S_0 = S_1 = 1$ can be used to facilitate transfer operations in an arithmetic section.

LOGIC DIAGRAM AND TRUTH TABLES

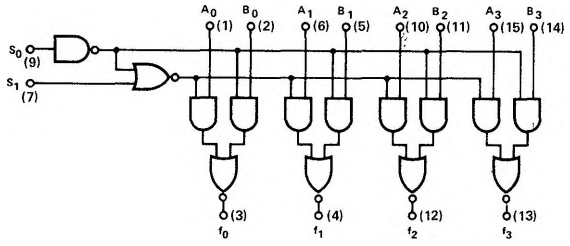
8233



S_0	S_1	f_n
0	0	B
1	0	A
0	1	B
1	1	0

V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

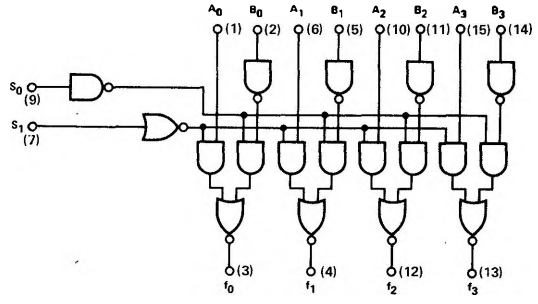
8234



S_0	S_1	f_n
0	0	$\overline{B}$
1	0	$\overline{A}$
0	1	$\overline{B}$
1	1	1

V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

8235



S_0	S_1	f_n
0	0	$\overline{A_n B_n}$
0	1	B_n
1	0	$\overline{A_n}$
1	1	1

V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS				OUTPUTS	NOTES
					INPUTS					
	MIN.	TYP.	MAX.	UNITS	A_n	B_n	S_0	S_1		
"1" Output Voltage (8233)	2.6	3.5		V	2.0V	2.0V	0.8V	0.8V	-800μA	6
"0" Output Voltage (8233)			0.4	V	0.8V	2.0V	2.0V	0.8V	16mA	7
"0" Output Voltage (8234)			0.4	V	0V	2.0V	0.8V	0.8V	16mA	7
"0" Output Voltage (8235)			0.4	V	2.0V	2.0V	2.0V	0.8V	16mA	7
"1" Output Leakage Current										
(8234)			100	μA	2.0V	2.0V	2.0V	2.0V	5.0V	13
"1" Output Leakage Current										
(8235)			100	μA	2.0V	2.0V	2.0V	2.0V	5.0V	13
"0" Input Current										
A_n	-0.1		-1.6	mA	0.4V	4.5V		0V		
B_n	-0.1		-1.6	mA	4.5V	0.4V	0V	0V		
S_0	-0.1		-1.6	mA			0.4V			
S_1	-0.1		-1.6	mA				0.4V		
"1" Input Current										
A_n			40	μA	4.5V	0V				
B_n			40	μA	0V	4.5V				
S_0			40	μA			4.5V			
S_1			40	μA				4.5V		
Input Latch Voltage										
A_n	5.5			V	10mA	0V				11
B_n	5.5			V	0V	10mA				11
S_0	5.5			V			10mA			11
S_1	5.5			V				10mA		11
Output Short Circuit Current										
(8233)	-20		-70	mA	5V	5V	0V	0V	0V	
Input Clamp Voltage										
A_n			-1.5	V	-12mA					
B_n			-1.5	V		-12mA				
S_0			-1.5	V			-12mA			
S_1			-1.5	V				-12mA		

$T_A = 25^\circ C$ and $V_{CC} = 5.0V$

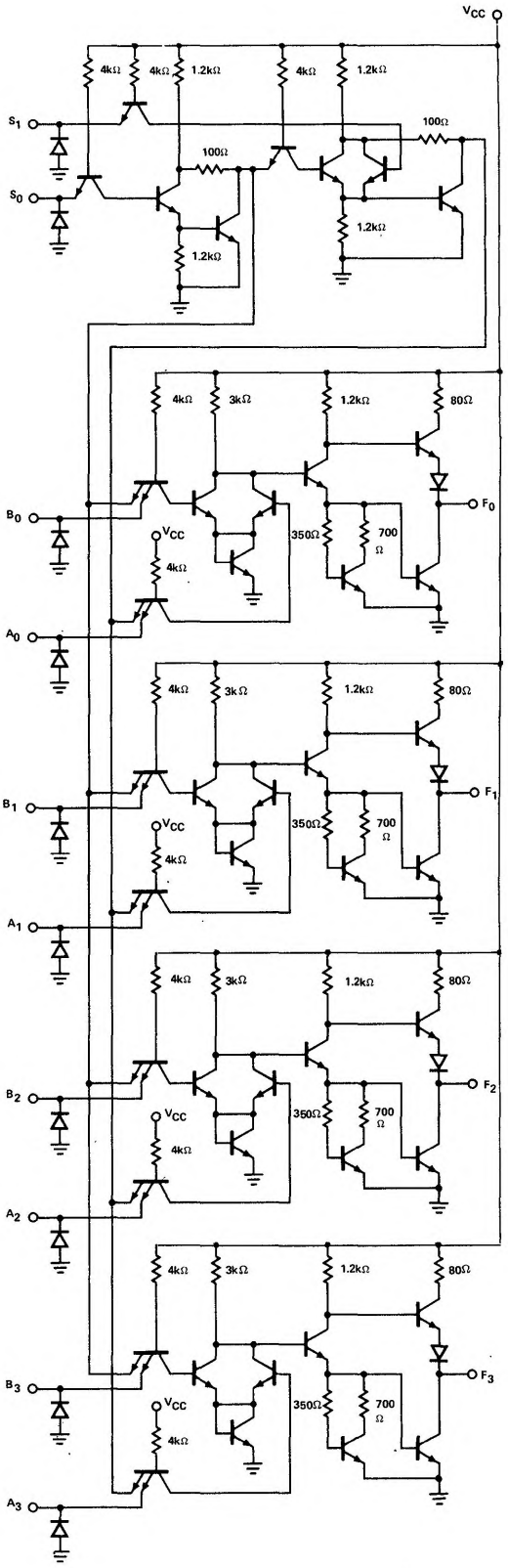
CHARACTERISTICS	LIMITS				TEST CONDITIONS				OUTPUTS	NOTES
					INPUTS					
	MIN.	TYP.	MAX.	UNITS	A_n	B_n	S_0	S_1		
Power/Current										
Consumption:										
8233		200/38	252/48	mW/mA		0V		0V		15
8234		160/31	210/40	mW/mA		0V		0V		15
8235		230/44	310/59	mW/mA		4.5V		4.5V		15
8233 Turn-On Times										
A_n, B_n to f_n		16	25	ns						8,14
S_0 to f_n		27	38	ns						8,14
S_1 to f_n		27	38	ns						8,14
8233 Turn-Off Times										
A_n, B_n to f_n		16	25	ns						8,14
S_0 to f_n		27	38	ns						8,14
S_1 to f_n		27	38	ns						8,14
8234 Turn-On Times										
A_n, B_n to f_n		16	25	ns						8,14
S_0 to f_n		27	38	ns						8,14
S_1 to f_n		27	38	ns						8,14
8234 Turn-Off Times										
A_n, B_n to f_n		16	25	ns						8,14
S_0 to f_n		27	38	ns						8,14
S_1 to f_n		27	38	ns						8,14
8235 Turn-On Times										
A_n to f_n		16	25	ns						8,14
B_n to f_n		24	35	ns						8,14
S_0 to f_n		27	38	ns						8,14
S_1 to f_n		27	38	ns						8,14
8235 Turn-Off Times										
A_n to f_n		16	25	ns						8,14
B_n to f_n		24	35	ns						8,14
S_0 to f_n		27	38	ns						8,14
S_1 to f_n		27	38	ns						8,14

NOTES:

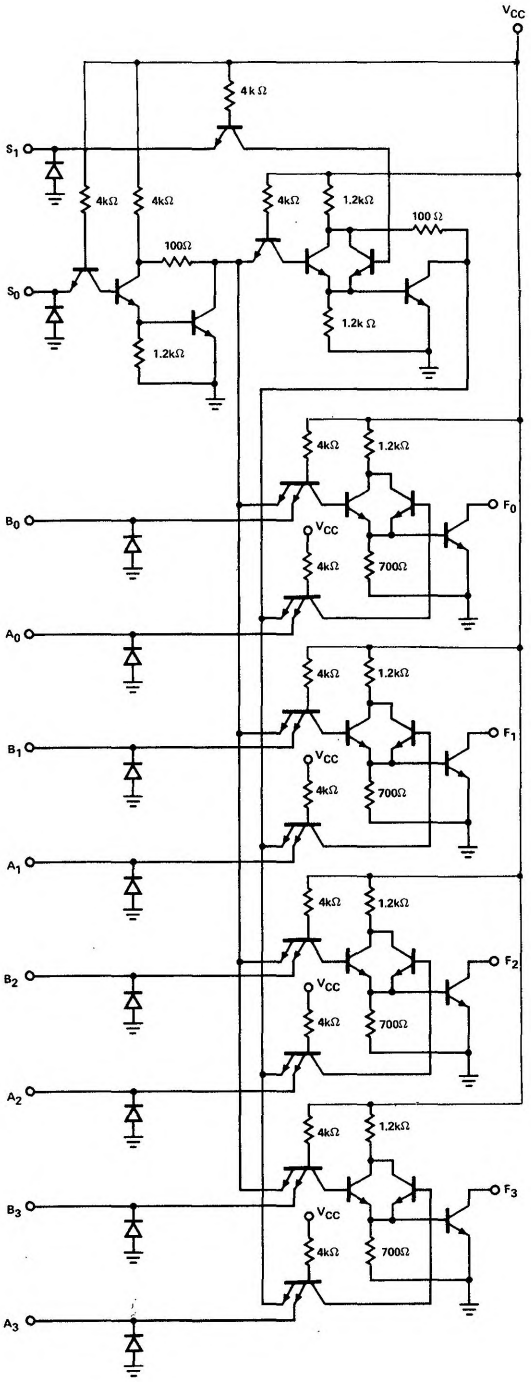
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. One DC fan-out is defined as 0.8mA.
9. One AC fan-out is defined as 50pF.
10. Manufacturer reserves the right to make design and process changes and improvements.
11. This test guarantees operation free of input latch-up within the specified operating supply voltage range.
12. Measurements apply to each gate element independently.
13. Connect an external 1k ±1% resistor from V_{CC} to the output for this test.
14. Reference AC Test Circuit, Waveforms and Test Tables.
15. $V_{CC} = 5.25V$.

SCHEMATIC DIAGRAMS

8233

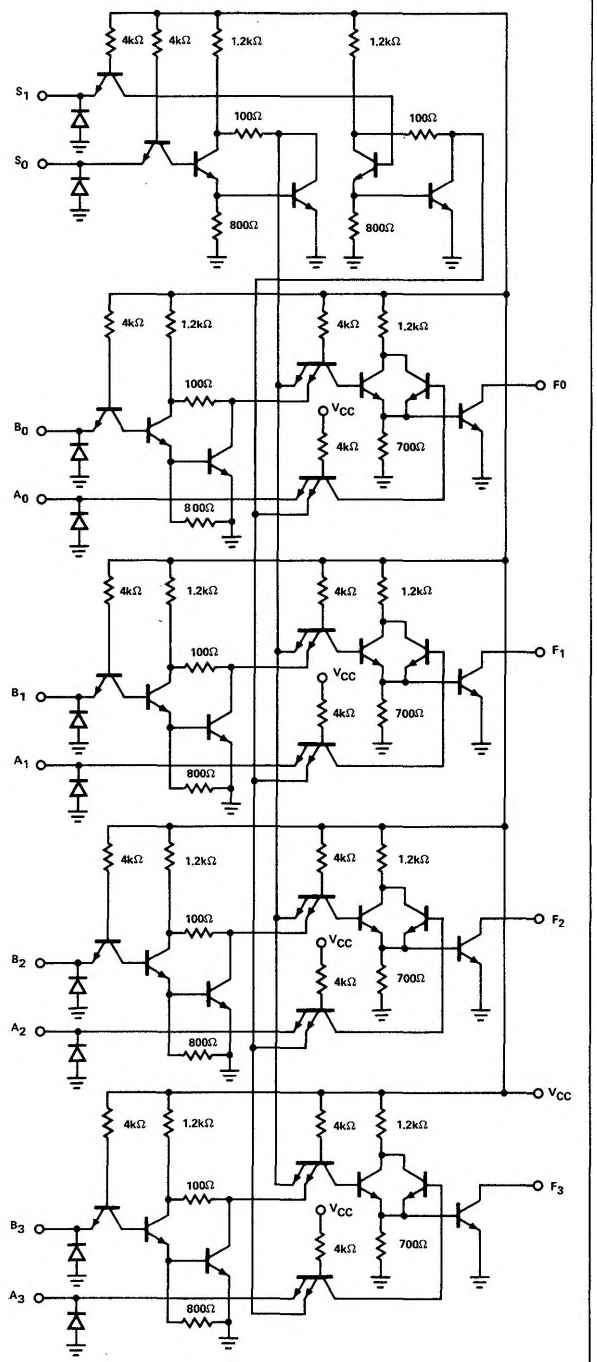


8234



SCHEMATIC DIAGRAMS (Cont'd)

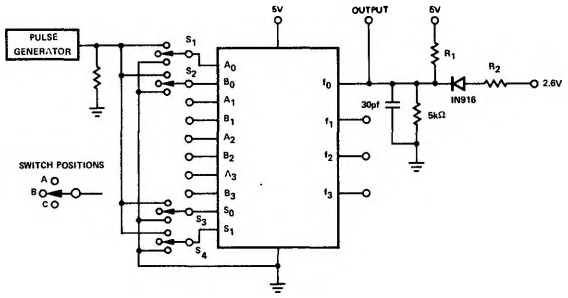
8235



PROPAGATION DELAY TEST TABLE

PRODUCT	PATH	PARAMETER	S_1	S_2	S_3	S_4
ALL	A_0 to f_0	$\frac{t_{on}}{t_{off}}$	a	b	b	c
8233 8234	B_0 to f_0	$\frac{t_{on}}{t_{off}}$	c	a	c	b
8233 8234	S_0 to f_0	$\frac{t_{on}}{t_{off}}$	b	b	a	b
8233 8234	S_0 to f_0	$\frac{t_{on}}{t_{off}}$	b	c	a	c
8235	B_0 to f_0	$\frac{t_{on}}{t_{off}}$	c	a	c	b
8235	B_0 to f_0	$\frac{t_{on}}{t_{off}}$	b	c	a	b
8235	S_1 to f_0	$\frac{t_{on}}{t_{off}}$	b	b	c	a
8233 8234	S_1 to f_0	$\frac{t_{on}}{t_{off}}$	b	c	b	a

AC TEST FIGURE AND WAVEFORMS



	R_1	R_2
8233	∞	84.5Ω
8234 8235	360Ω	440Ω

INPUT PULSE:
Amplitude = 2.6V
PW = 200ns
PRR = 1 MHz
$t_r = t_f = 5ns$

PULSE REQUIREMENTS