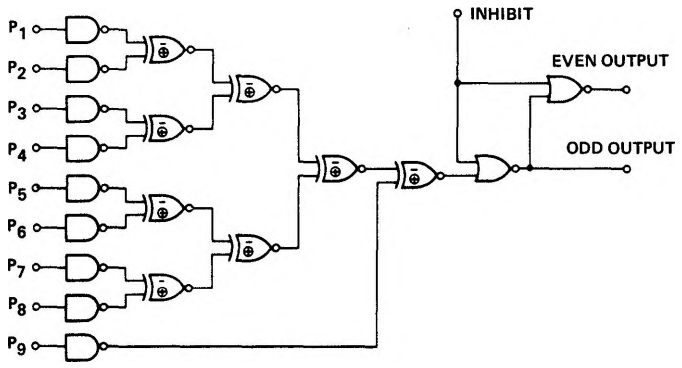
DESCRIPTION

The 8262 9-Input Parity Generator/Parity Checker is a versatile MSI device commonly used to detect errors in data transmission or in data retrieval. Two outputs (EVEN and ODD) are provided for versatility. An INHIBIT input is provided to disable both outputs of the 8262. (A logic 1 on the INHIBIT input forces both outputs to a logic 0).

When used as a Parity Generator, the 8262 supplies a parity bit which is transmitted together with the data word.

At the receiving end, the 8262 acts as a Parity Checker and indicates that data has been received correctly or that an error has been detected.

LOGIC DIAGRAM



LOGIC EQUATIONS:

Odd =

$$P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9$$

Even =

$$\overline{P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9}$$

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS	INHIBIT	OUTPUTS UNDER TEST	NOTES
	MIN.	TYP.	MAX.	UNITS	DATA INPUT UNDER TEST			
"1" Output Voltage								
Even	2.6	3.5		V	0V	.8V	-800μA	6
Odd	2.6	3.5		V	2.0V	.8V	-800μA	6
"0" Output Voltage								
Even			0.40	V	2.0V	.8V	16mA	7
Odd			0.40	V	0V	.8V	16mA	7
"0" Input Current								
Data Inputs	-0.1		-1.6	mA	0.4V			
Inhibit	-0.1		-3.2	mA		0.4V		
"1" Input Current								
Data Inputs			80	μA	4.5V			
Inhibit			160	μA		4.5V		
Input Latch Voltage								
Data Inputs	5.5			V	10mA			10
Inhibit	5.5			V		10mA		10
Power/Current Consumption			370/70	mW/mA				11
Output Short Circuit Current								
Even	-20		-70	mA	0V	0V	0V	
Odd	-20		-70	mA	4.5V	0V	0V	

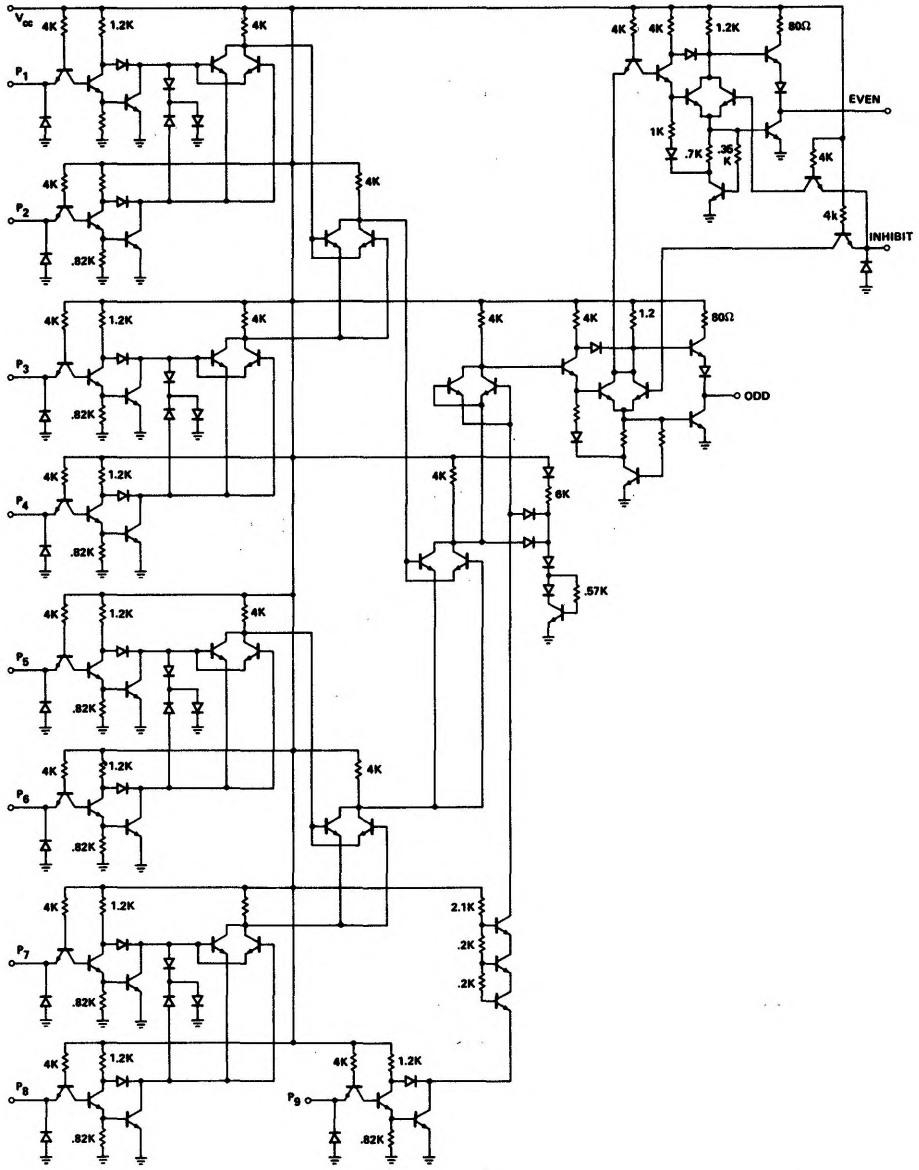
$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS	INHIBIT	OUTPUTS UNDER TEST	NOTES
	MIN.	TYP.	MAX.	UNITS	UNDER TEST			
Turn-On Times								
$P_1 - P_8$ to Even		35	50	ns	Pulse			8
$P_1 - P_8$ to Odd		30	45	ns	Pulse			8
P_9 to Even		20	35	ns	Pulse			8
P_9 to Odd		15	30	ns	Pulse			8
Inhibit to Even		8	15	ns		Pulse		8
Inhibit to Odd		8	15	ns		Pulse		8
Turn-Off Times								
$P_1 - P_8$ to Even		38	55	ns	Pulse			8
$P_1 - P_8$ to Odd		32	45	ns	Pulse			8
P_9 to Even		23	40	ns	Pulse			8
P_9 to Odd		20	35	ns	Pulse			8
Inhibit to Even		10	18	ns		Pulse		8
Inhibit to Odd		10	18	ns		Pulse		8

NOTES:

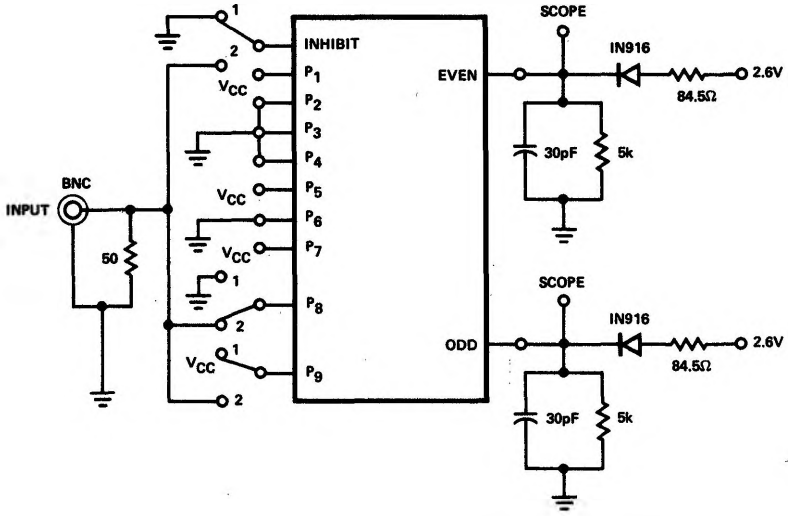
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figure.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
11. V_{CC} = 5.25 volts.

SCHEMATIC DIAGRAM

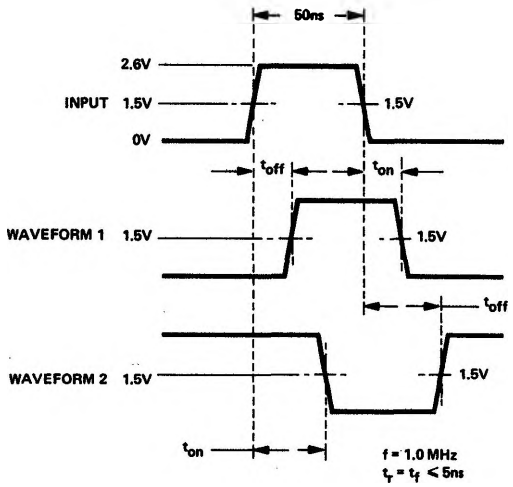


AC TEST FIGURE AND WAVEFORMS

8262 PARITY GENERATOR-CHECKER



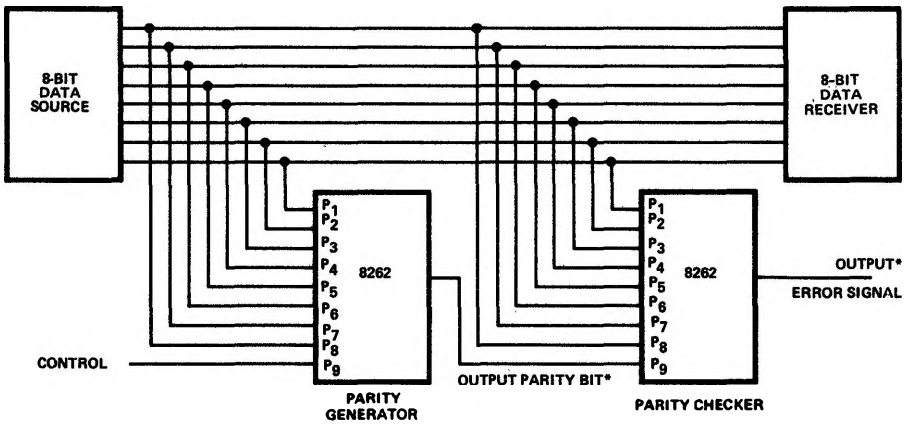
PULSE REQUIREMENTS



TRUTH TABLE

MEASURE DELAY FROM	SWITCH POSITION			WAVEFORM	
	INH	P_8	P_9	EVEN	ODD
P_8 to ODD	1	2	1		1
P_9 to ODD	1	1	2		2
P_8 to EVEN	1	2	1	2	
P_9 to EVEN	1	1	2	1	
INH to EVEN	2	1	1	2	

TYPICAL APPLICATIONS



*Output can be conditioned for odd or even parity.

An "even parity bit" checking code has a parity bit such that the sum of the 1's in the data word plus the parity bit is always an even number.

An "odd parity bit" checking code has a parity bit such that the sum of the 1's in the data word plus the parity bit is always an odd number.