## DESCRIPTION

The 82S66/82S67 2-Input, 4-Bit Digital Multiplexer is a monolithic array utilizing Schottky TTL circuit structures. The 82S67 features a bare-collector output to allow expansion with other devices.

The multiplexer is intended for use at the inputs to adders, registers and in other parallel data handling applications.

The multiplexer is able to choose from two different input sources, each containing 4 bits: A = ($A_0$, $A_1$, $A_2$, $A_3$), B = ($B_0$, $B_1$, $B_2$, $B_3$). The selection is controlled by the input $S_0$, while the second control input, $S_1$, is held at zero.

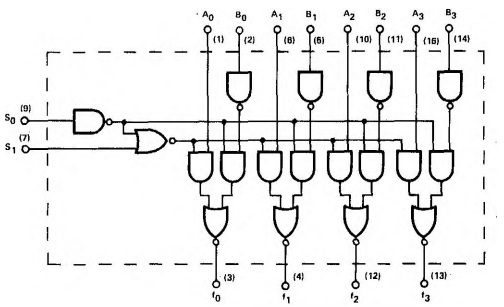
For conditional complementing, the two inputs ($A_n$, $B_n$) are tied together to form the function TRUE/COMPLEMENT, which is needed in conjunction with adder elements to perform ADDITION/SUBTRACTION. Further, the inhibit state $S_0 = S_1 = 1$ can be used to facilitate transfer operations in an arithmetic section.

## FEATURES

- SCHOTTKY-CLAMPED TTL STRUCTURE
- PNP INPUTS
- OPEN COLLECTOR OUTPUTS (82S67)
- INHIBIT STATE

## LOGIC DIAGRAM AND TRUTH TABLE

**82S66/82S67**




$V_{CC}$ = (16)
GND = (8)
( ) = Denotes Pin Numbers

| SELECT LINES | | OUTPUTS |
|---|---|---|
| $S_0$ | $S_1$ | $f_n$ (0, 1, 2, 3) |
| 0 | 0 | $B_n$ |
| 0 | 1 | $\overline{B}_n$ |
| 1 | 0 | $\overline{A}_n$ |
| 1 | 1 | 1 |

## ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature and Voltage)

| CHARACTERISTICS | LIMITS | | | | TEST CONDITIONS | | | | | NOTES |
|---|---|---|---|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | UNITS | $A_n$ | $B_n$ | $S_0$ | $S_1$ | OUTPUTS | |
| "1" Output Voltage (82S66) | 2.7 | 3.5 | | V | 0.8V | 2.0V | 0.8V | 0.8V | −1mA | 7 |
| "0" Output Voltage | | | 0.5 | V | 2.0V | 2.0V | 2.0V | 0.8V | 20mA | 8 |
| "1" Output Leakage Current (82S67) | | | 250 | μA | 0.8V | 2.0V | 2.0V | 0.8V | 5.5V | |
| "0" Input Current | | | | | | | | | | |
| $A_n$, $B_n$ | | | −400 | μA | 0.5V | 0.5V | 0V | 0V | | |
| $S_0$, $S_1$ | | | −400 | μA | | | 0.5V | 0.5V | | |
| "1" Input Current | | | | | | | | | | |
| $A_n$, $B_n$ | | | 10 | μA | 4.5V | 4.5V | | 2.0V | | |
| $S_0$, $S_1$ | | | 10 | μA | | | 4.5V | 4.5V | | |
| Output Short Circuit Current (82S66) | −40 | | −100 | mA | | | | | | 12 |

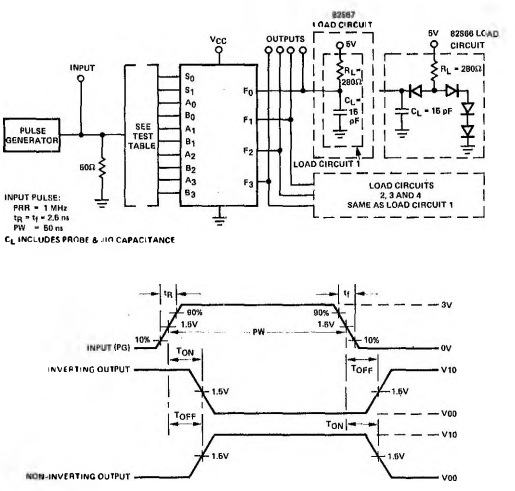
## $T_A = 25^oC$ and $V_{CC} = 5.0V$

| CHARACTERISTICS | LIMITS | | | | TEST CONDITIONS | | | | | NOTES |
|---|---|---|---|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | UNITS | $A_n$ | $B_n$ | $S_0$ | $S_1$ | OUTPUTS | |
| Turn-on/Turn-off Times (82S66) | | | | | | | | | | |
| $S_1$ to $f_n$ | | | 15 | ns | | | | | | 9 |
| $S_0$ to $f_n$ | | | 18 | ns | | | | | | 9 |
| $A_n$ to $f_n$ | | | 10 | ns | | | | | | 9 |
| $B_n$ to $f_n$ | | | 12 | ns | | | | | | 9 |
| Propagation Delay (82S67) | | | | | | | | | | |
| $S_1$ to $f_n$ | | | 18 | ns | | | | | | 9 |
| $S_0$ to $f_n$ | | | 20 | | | | | | | |
| $A_n$ to $f_n$ | | | 12 | ns | | | | | | 9 |
| $B_n$ to $f_n$ | | | 15 | ns | | | | | | 9 |
| Power/Current Consumption | | | 365/69 | mW/mA | 4.5V | 0V | 4.5V | 0V | | 12 |

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to $V_{CC}$.
9. Refer to AC Test Figure.
10. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
11. Manufacturer reserves the right to make design and process changes and improvements.
12. $V_{CC}$ = 5.25 V.

## AC TEST FIGURE AND WAVEFORMS




| TEST NO. | INPUTS | | | | | | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $S_0$ | $S_1$ | $A_0$ | $B_0$ | $A_1$ | $B_1$ | $A_2$ | $B_2$ | $A_3$ | $B_3$ | $F_0$ | $F_1$ | $F_2$ | $F_3$ |
| 1 | 1 | PG | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | T | | | |
| 2 | 1 | PG | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | T | T | T | T |
| 3 | PG | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | T | | | T |
| 4 | 0 | 0 | 0 | 0 | PG | 0 | 0 | 0 | 0 | | | T | | |
| 5 | 0 | 0 | 0 | 0 | 0 | 0 | PG | 0 | 0 | | | | T | |
| 6 | 1 | 0 | PG | 1 | 0 | 1 | 0 | 1 | 0 | 1 | T | | | |
| 7 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | PG | 1 | | | | T |

"1" = 2.7V "0" = OUTPUT

NOTE:
1. A.C. TEST JIGS MUST NOT HAVE ANY SWITCHES.
2. A.C. TEST JIGS MUST HAVE LESS THAN 1/8 INCH LEAD LENGTH FROM PACKAGE PINS.