SIGNETICS DCL INTEGRATED CIRCUITS

8424 DUAL RS/T BINARY

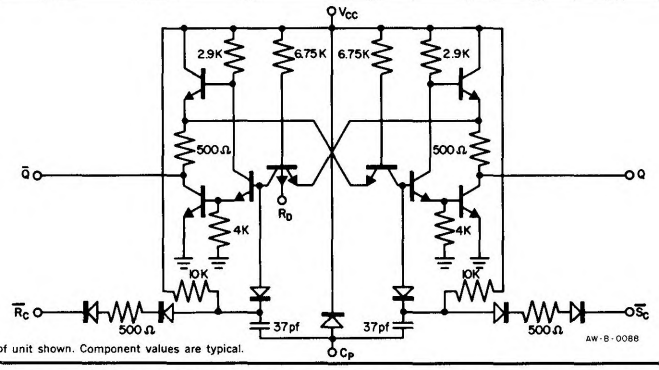
The 8424 is a low power, capacitively coupled Dual RS/T Binary.

This element responds to the trailing or negative-going transition of the clock pulse. The asynchronous RESET input, $\overline{R}_D$, may be activated independent of the state of the clock. The synchronous inputs ($\overline{R}_C$ and $\overline{S}_C$) are especially adaptable to NAND logic systems since they respond to low levels. The $\overline{R}_C$ and $\overline{S}_C$ inputs have no effect when the clock line is stationary.

Each logic element in the 8000 series is characterized to provide guarantees for driving the 8424. A convenient summary of these AC loading rules is provided in Table 1-5, Section 1.

Usage rules and applications information and suggestions are included in Section 4 of this handbook.

BASIC CIRCUIT SCHEMATIC



NOTE: ½ of unit shown. Component values are typical.

TRUTH TABLE

$\overline{R}_{Cn}$	$\overline{S}_{Cn}$	Q_{n+1}
1	0	1
0	1	0
1	1	Q
0	0	?

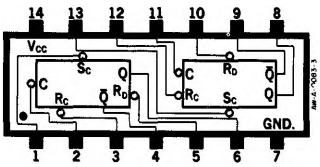
$\overline{R}_D = 0 \Rightarrow Q = 0$

n is time prior to clock
n+1 is time following clock

ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 15)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	TEST LIMITS				TEST CONDITIONS								
		MIN.	TYP.	MAX.	UNITS	TEMP. S8424	TEMP. N8424	V_{cc}	$\overline{R}_D$	CLOCK	$\overline{R}_C$	$\overline{S}_C$	OUTPUT	NOTES
A-5	"1" OUTPUT VOLTAGE (Q)	3.4			V	-55°C	0°C	4.75V	2.0V				-225µA	12, 8
A-3	(Q)	3.6			V	+25°C	+25°C	5.0V	2.0V				-225µA	12, 8
A-4	(Q)	3.4			V	+125°C	+75°C	4.75V	2.0V				-225µA	12, 8
A-5	"1" OUTPUT VOLTAGE ($\overline{Q}$)	3.4			V	-55°C	0°C	4.75V	0.7V				-225µA	8
A-3	($\overline{Q}$)	3.6			V	+25°C	+25°C	5.0V	0.7V				-225µA	8
A-4	($\overline{Q}$)	3.4			V	+125°C	+75°C	4.75V	0.7V				-225µA	8
A-5	"0" OUTPUT VOLTAGE (Q)			0.35	V	-55°C	0°C	4.75V	0.7V				7.2mA	9
A-3	(Q)			0.35	V	+25°C	+25°C	5.0V	0.7V				7.2mA	9
A-4	(Q)			0.35	V	+125°C	+75°C	4.75V	0.7V				7.2mA	9
A-5	"0" OUTPUT VOLTAGE ($\overline{Q}$)			0.35	V	-55°C	0°C	4.75V	2.0V				7.2mA	12, 9
A-3	($\overline{Q}$)			0.35	V	+25°C	+25°C	5.0V	2.0V				7.2mA	12, 9
A-4	($\overline{Q}$)			0.35	V	+125°C	+75°C	4.75V	2.0V				7.2mA	12, 9
C-1	"0" INPUT CURRENT ($\overline{R}_D$)	-0.1		-0.8	mA	-55°C	0°C	5.25V	0.35V					13
A-3		-0.1		-0.8	mA	+25°C	+25°C	5.25V	0.35V					13
C-1		-0.1		-0.8	mA	+125°C	+75°C	5.25V	0.35V					13
C-1	"0" INPUT CURRENT ($\overline{R}_C$, $\overline{S}_C$)	-0.1		-0.6	mA	-55°C	0°C	5.25V			0.35V	0.35V		
A-3		-0.1		-0.6	mA	+25°C	+25°C	5.25V			0.35V	0.35V		
C-1		-0.1		-0.6	mA	+125°C	+75°C	5.25V			0.35V	0.35V		
A-4	"0" INPUT CURRENT (CLOCK)			25	µA	+125°C	+75°C	5.25V		0V				
A-4	"1" INPUT CURRENT ($\overline{R}_D$)			25	µA	+125°C	+75°C	4.75V	4.5V					14
A-4	"1" INPUT CURRENT ($\overline{R}_C$, $\overline{S}_C$)			25	µA	+125°C	+75°C	4.75V			4.5V	4.5V		
A-6	CLOCKED MODE HOLDING TEST (C)			10	ns	+25°C	+25°C	5.0V		PULSE				16
A-6	CLOCKED MODE SWITCHING TEST (C)			50	ns	+25°C	+25°C	5.0V		PULSE				16
A-6	(C)			75	ns	+25°C	+25°C	5.0V		PULSE				
A-6	CLOCKED MODE TURN-ON DELAY			60	ns	+25°C	+25°C	5.0V					D.C.F.O. = 9	10, 16
A-6	CLOCKED MODE TURN-OFF DELAY			60	ns	+25°C	+25°C	5.0V					D.C.F.O. = 9	10, 16
A-6	TOGGLE RATE	8			MHz	+25°C	+25°C	5.0V			$\overline{Q}$	Q		16
C-2	OUTPUT FALL TIME			75	ns	-55°C	0°C	4.75V					A.C.F.O. = 2	11, 16
C-2	INPUT CAPACITANCE (CLOCK)			50	pf	+25°C	+25°C	5.0V		2.0V				7
C-2	($\overline{R}_D$)			3.0	pf	+25°C	+25°C	5.0V	2.0V					7
C-2	($\overline{R}_C$, $\overline{S}_C$)			3.0	pf	+25°C	+25°C	5.0V			2.0V	2.0V		7
A-2	POWER CONSUMPTION (PER BINARY)			24.7	mW	+25°C	+25°C	5.25V			$\overline{Q}$	Q		
A-2	INPUT VOLTAGE RATING (CLOCK)	5.0		6.0	V	+25°C	+25°C	5.0V		10µA	0V	0V		
	($\overline{R}_D$)	5.5			V	+25°C	+25°C	5.0V	50µA					14
	($\overline{R}_C$, $\overline{S}_C$)	5.5			V	+25°C	+25°C	5.0V		0V	10µA	10µA		
A-2	OUTPUT SHORT CIRCUIT CURRENT ($\overline{Q}$)	-5.0		-12.0	mA	+25°C	+25°C	5.0V	0V				0V	

A PACKAGE



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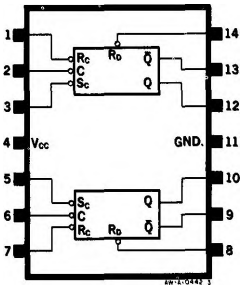

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Notes:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to V_{CC}.
10. One DC fan-out is defined as 0.8mA.
11. One AC fan-out is defined as 50pf.
12. Momentarily apply zero volts to $\bar{Q}$ and V_{CC} to Q to ensure the state of the flip-flop prior to measurement.
13. Apply 0.5V to the Q output terminal.
14. Apply V_{CC} to $\bar{Q}$ output terminal and zero volts to Q output terminal.
15. Manufacturer reserves the right to make design and process changes and improvements.
16. Detailed test conditions for AC testing are in Section 3.