SIGNETICS DCL INTEGRATED CIRCUITS

8425 DUAL RS/T BINARY

The 8425 is a low-power, capacitively coupled Dual RS/T AC Binary.

This element responds to the trailing or negative-going transition of the clock pulse and features a common-clock, common RESET ($\overline{R}_D$) and separate SET ($\overline{S}_D$) which provide maximum usage of all inputs in synchronous systems such as shift registers and synchronous counters. The asynchronous RESET inputs, $\overline{R}_D/\overline{S}_D$, may be activated independent of the state of the clock, thus providing random access to synchronous systems. The synchronous inputs ($\overline{R}_C$ and $\overline{S}_C$) are especially adaptable to NAND logic systems since they respond to low levels. The $\overline{R}_C$ and $\overline{S}_C$ inputs have no effect when the clock line is stationary.

Each logic element in the 8000 series is characterized to provide guarantees for driving the 8425. A convenient summary of these AC loading rules is provided in Table 1-5, Section 1.

Usage rules and applications information are included in Section 4 of this handbook.

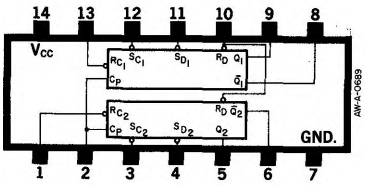
ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 15)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS			TEST CONDITIONS									
		MIN.	MAX.	UNITS	TEMP. S8425	TEMP. N8425	V_{cc}	$\overline{S}_D$	$\overline{R}_D$	CLOCK	$\overline{R}_C$	$\overline{S}_C$	OUTPUTS	NOTES
A-5	"1" OUTPUT VOLTAGE (Q)	3.4		V	-55°C	0°C	4.75V	0.7V	2.0V				-225μA	8
A-3	(Q)	3.6		V	+25°C	+25°C	5.0V	0.7V	2.0V				-225μA	8
A-4	(Q)	3.4		V	+125°C	+75°C	4.75V	0.7V	2.0V				-225μA	8
A-5	"1" OUTPUT VOLTAGE ($\overline{Q}$)	3.4		V	-55°C	0°C	4.75V	2.0V	0.7V				-225μA	8
A-3	($\overline{Q}$)	3.6		V	+25°C	+25°C	5.0V	2.0V	0.7V				-225μA	8
A-4	($\overline{Q}$)	3.4		V	+125°C	+75°C	4.75V	2.0V	0.7V				-225μA	8
A-5	"0" OUTPUT VOLTAGE (Q)		0.35	V	-55°C	0°C	4.75V	2.0V	0.7V				7.2mA	9
A-3	(Q)		0.35	V	+25°C	+25°C	5.0V	2.0V	0.7V				7.2mA	9
A-4	(Q)		0.35	V	+125°C	+75°C	4.75V	2.0V	0.7V				7.2mA	9
A-5	"0" OUTPUT VOLTAGE ($\overline{Q}$)		0.35	V	-55°C	0°C	4.75V	0.7V	2.0V				7.2mA	9
A-3	($\overline{Q}$)		0.35	V	+25°C	+25°C	5.0V	0.7V	2.0V				7.2mA	9
A-4	($\overline{Q}$)		0.35	V	+125°C	+75°C	4.75V	0.7V	2.0V				7.2mA	9
C-1	"0" INPUT CURRENT ($\overline{R}_D$)	-0.1	-1.6	mA	-55°C	0°C	5.25V		0.35V					12
A-3	($\overline{R}_D$)	-0.1	-1.6	mA	+25°C	+25°C	5.25V		0.35V					12
C-1	($\overline{R}_D$)	-0.1	-1.6	mA	+125°C	+75°C	5.25V		0.35V					12
C-1	"0" INPUT CURRENT ($\overline{S}_D$)	-0.1	-0.8	mA	-55°C	0°C	5.25V	0.35V						12
A-3	($\overline{S}_D$)	-0.1	-0.8	mA	+25°C	+25°C	5.25V	0.35V						12
C-1	($\overline{S}_D$)	-0.1	-0.8	mA	+125°C	+75°C	5.25	0.35V						12
C-1	"0" INPUT CURRENT ($\overline{R}_C$, $\overline{S}_C$)	-0.1	-0.6	mA	-55°C	0°C	5.25V				0.35V	0.35V		
A-3	($\overline{R}_C$, $\overline{S}_C$)	-0.1	-0.6	mA	+25°C	+25°C	5.25V				0.35V	0.35V		
C-1	($\overline{R}_C$, $\overline{S}_C$)	-0.1	-0.6	mA	+125°C	+75°C	5.25V				0.35V	0.35V		
A-4	"0" INPUT CURRENT (CLOCK)		-50	μA	+125°C	+75°C	5.25V			0V				
A-4	"1" INPUT CURRENT ($\overline{S}_D$)		25	μA	+125°C	+75°C	4.75V	4.5V						13
A-3	($\overline{S}_D$)		25	μA	+25°C	+25°C	4.75V	4.5V						13
A-4	($\overline{R}_D$)		50	μA	+125°C	+75°C	4.75V		4.5V					13
A-3	($\overline{R}_D$)		50	μA	+25°C	+25°C	4.75V		4.5V					13
A-6	CLOCKED MODE HOLDING TEST		10	ns	+25°C	+25°C	5.0V			PULSE				15
A-6	CLOCKED MODE SWITCHING TEST		50	ns	+25°C	+25°C	5.0V			PULSE				15
A-6			75	ns	+25°C	+25°C	5.0V			PULSE				15
A-6	CLOCKED MODE TURN-ON DELAY		60	ns	+25°C	+25°C	5.0V						D.C.F.O. = 9	10, 15
A-6	CLOCKED MODE TURN-OFF DELAY		60	ns	+25°C	+25°C	5.0V						D.C.F.O. = 9	10, 15
A-6	TOGGLE RATE	8		MHz	+25°C	+25°C	5.0V				$\overline{Q}$	Q		15
C-2	OUTPUT FALL TIME		75	ns	-55°C	0°C	4.75V						A.C.F.O. = 2	11, 15
C-2	INPUT CAPACITANCE (CLOCK)		100	pf	+25°C	+25°C	5.0V			2.0V				7
C-2	($\overline{S}_D$)		3.0	pf	+25°C	+25°C	5.0V	2.0V						7
C-2	($\overline{R}_D$)		6.0	pf	+25°C	+25°C	5.0V		2.0V					7
C-2	($\overline{R}_C$, $\overline{S}_C$)		3.0	pf	+25°C	+25°C	5.0V				2.0V	2.0V		7
A-2	POWER CONSUMPTION (Per Binary)		24.7	mW	+25°C	+25°C	5.25V				$\overline{Q}$	Q		
A-2	INPUT VOLTAGE RATING (CLOCK)	5.0	6.0	V	+25°C	+25°C	5.0V			10μA	0V	0V		
A-2	($\overline{S}_D$, $\overline{R}_D$)	5.5		V	+25°C	+25°C	5.0V	50μA	50μA					13
A-2	($\overline{R}_C$, $\overline{S}_C$)	5.5		V	+25°C	+25°C	5.0V			0V	10μA	10μA		
A-2	OUTPUT SHORT CIRCUIT CURRENT ($\overline{Q}$)	-5.0	-12	mA	+25°C	+25°C	5.0V		0V				0V	
A-2	(Q)	-5.0	-12	mA	+25°C	+25°C	5.0V	0V					0V	

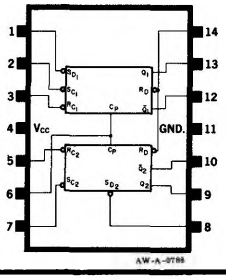
Notes:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV rms. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to V_{cc}.
10. One DC fan-out is defined as 0.8mA.
11. One AC fan-out is defined as 50pf.
12. Apply 0.5V to the Q output terminal for $\overline{R}_D$ test and 0.5V to $\overline{Q}$ for $\overline{S}_D$ test.
13. Apply V_{cc} to $\overline{Q}$ output terminal and zero volts to Q output terminal for $\overline{R}_D$ test and V_{cc} to Q and zero volts to $\overline{Q}$ for $\overline{S}_D$ test.
14. Manufacturer reserves the right to make design and process changes and improvements.
15. Detailed test conditions for AC testing are in Section 3.

A PACKAGE



J PACKAGE



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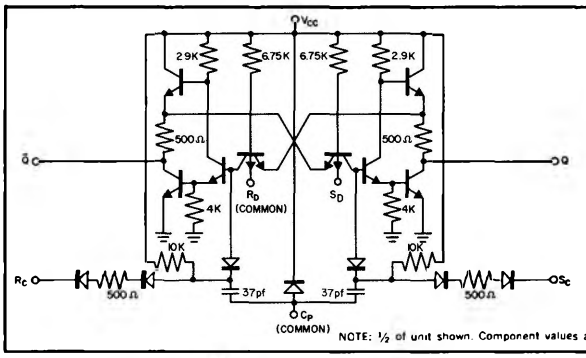
BASIC CIRCUIT SCHEMATIC



NOTE: ½ of unit shown. Component values are typical.

TRUTH TABLE

$\overline{R}_{C_n}$	$\overline{S}_{C_n}$	Q_{n+1}
1	0	1
0	1	0
1	1	Q
0	0	?

n is time prior to clock

$\overline{R}_D$	$\overline{S}_D$	Q
1	0	1
0	1	0
1	1	Q
0	0	*

*Both outputs go to "1" state until R_D or S_D rises.