SIGNETICS

DCL

INTEGRATED CIRCUITS

8440 DUAL AND-OR-INVERT GATE

The 8440 Dual AND-OR-INVERT Gate implements the Exclusive-OR function.

The active output structure of the 8440 provides high AC noise immunity due to its low output impedance in both the "1" and "0" output states.

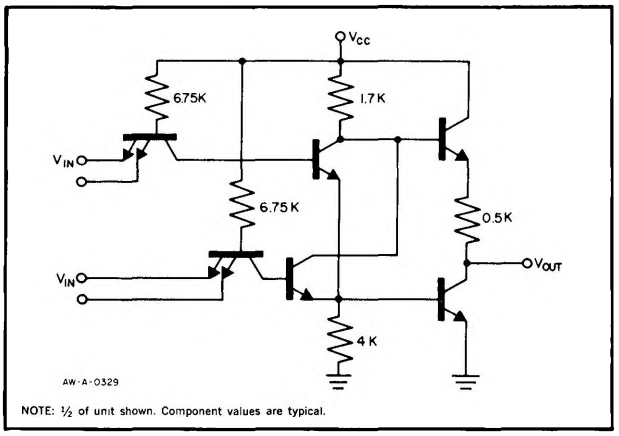
Output short circuit protection is provided by a current limiting resistor.

Values chosen for the collector and emitter resistors of the phase-splitter transistor ensure optimum on-off relationships of the totem-pole output pair.

General areas of application for the 8440 include half and full adders, digital comparators, and AND-OR control logic for inputs to binary clock steering lines.

Section 4 of this handbook contains helpful applications information and usage rules for the 8440.

BASIC CIRCUIT SCHEMATIC



NOTE: ½ of unit shown. Component values are typical.

ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 14)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8440	TEMP. N8440	V_{cc}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-5	"1" OURPUT VOLTAGE	3.4			V	-55°C	0°C	4.75V	0.7V		-225μA	8
A-3		3.6			V	+25°C	+25°C	5.0V	0.7V		-225μA	8
A-4		3.4			V	+125°C	+75°C	4.75V	0.7V		-225μA	8
A-5	"0" OUTPUT VOLTAGE			0.35	V	-55°C	0°C	4.75V	2.0V	2.0V	7.2mA	9, 12
A-3				0.35	V	+25°C	+25°C	5.0V	2.0V	2.0V	7.2mA	9, 12
A-4				0.35	V	+125°C	+75°C	4.75V	2.0V	2.0V	7.2mA	9, 12
C-1	"0" INPUT CURRENT	-0.1		-0.8	mA	-55°C	0°C	5.25V	0.35V	5.25V		
A-3		-0.1		-0.8	mA	+25°C	+25°C	5.25V	0.35V	5.25V		
C-1		-0.1		-0.8	mA	+125°C	+75°C	5.25V	0.35V	5.25V		
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	4.5V	0V		
A-6	PAIR DELAY	30		95	ns	+25°C	+25°C	5.0V			D.C.F.O. = 9	10, 15
C-2	OUTPUT FALL TIME			75	ns	-55°C	0°C	4.75V			A.C.F.O. = 2	11, 15
C-2	TURN-ON DELAY			40	ns	+25°C	+25°C	5.0V			D.C.F.O. = 9	10, 15
C-2	TURN-OFF DELAY			50	ns	+25°C	+25°C	5.0V			D.C.F.O. = 1	10, 15
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V			7
A-2	POWER CONSUMPTION OUTPUT "0"			29.4	mW	+25°C	+25°C	5.25V				
	(Per Gate) OUTPUT "1"			9.5	mW	+25°C	+25°C	5.25V	0V			13
A-2	INPUT VOLTAGE RATING	5.5			V	+25°C	+25°C	5.0V	50μA	0V		
A-2	OUTPUT SHORT CIRCUIT CURRENT	-4.0		-12	mA	+25°C	+25°C	5.0V	0V		0V	

Notes:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1 MHz, V_{ac} = 25mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor to ground. Apply 0.7V to one input terminal of associated AND gate.
9. Output sink current is supplied through a resistor to V_{cc}.
10. One DC fan-out is defined as 0.8mA.
11. One AC fan-out is defined as 50pf.
12. To test "0" output voltage, apply 2.0V to the input terminal of one input AND gate and apply zero volts to the input terminals of the associated input AND gate. Reverse input conditions and measure again.
13. For output "1" power consumption test, apply zero volts to one input terminal of associated input AND gates.
14. Manufacturer reserves the right to make design and process changes and improvements.
15. Detailed test conditions for AC testing are in Section 3.

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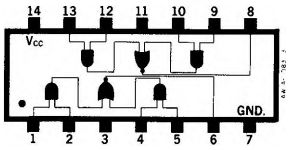

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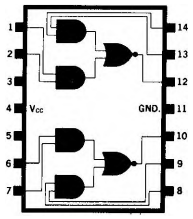

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