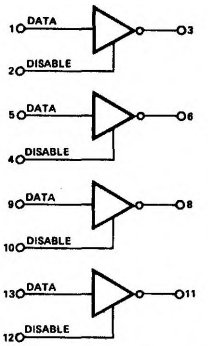
DESCRIPTION

The 8T09 is a high speed quad bus driver device for applications requiring up to 25 loads interconnected on a single bus.

The tri-state outputs present a high impedance to the bus when disabled, (control input "1") and active drive when enabled (control input "0"). This eliminates the resistor pull-up requirement while providing performance superior to open collector schemes. Each output can sink 40mA and drive 300pF loading with guaranteed propagation delay less than 22 nanoseconds.

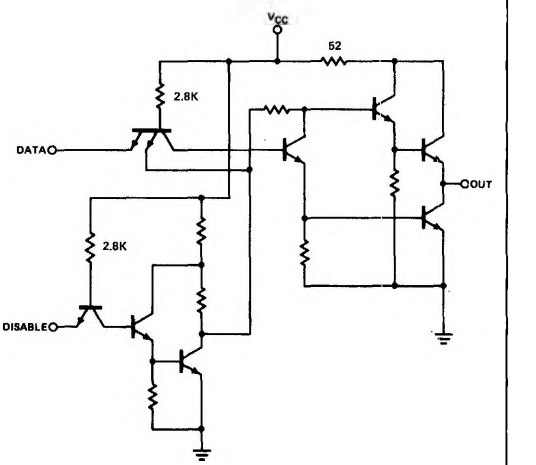
LOGIC DIAGRAM AND TRUTH TABLE



Data	Disable	Output
0	0	1
1	0	0
0	1	Hi- Z
1	1	Hi- Z

V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers for 14 Pin Dual-in-Line Package

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
	MIN.	TYP.	MAX.	UNITS	DATA	DISABLE	OUTPUTS	
"1" Output Voltage	2.4	3.0		V	0.8V	0.8V	-5.2mA	7
"0" Output Voltage		0.2	0.4	V	2.0V	0.8V	40mA	8
Output Leakage Current	-40		+40	μA		2.0V	0.4V or 2.4V	3
"1" Input Current			40	μA		4.5V		
"0" Input Current			-2.0	mA	0.4V	0.4V		
Input Voltage Rating	5.5			V	10mA	10mA		
Power/Current Consumption		236/45	340/65	mW/mA				11
Output Short Circuit Current	-40		-120	mA	0V	0V	0V	10, 11

T_A = 25° C and V_{CC} = 5.0V

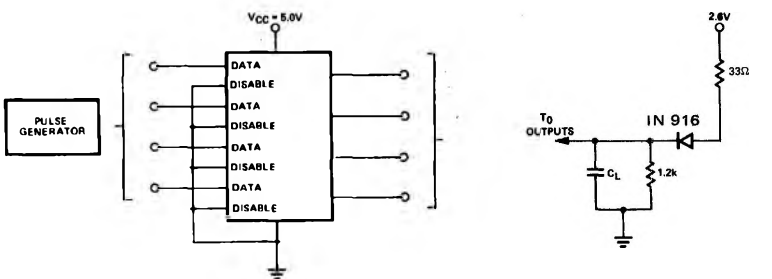
CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
	MIN.	TYP.	MAX.	UNITS	DATA	DISABLE	OUTPUTS	
Propagation Delay								
Data to Output								
t_{on}, t_{off}			10	ns			30pF load	9
			20	ns			300pF load	9
Disable to Output								
High Z to 0, 0 to High Z			14	ns			30pF load	9
			22	ns			300pF load	9
High Z to 1, 1 to High Z			14	ns			30pF load	9
			22	ns			300pF load	9

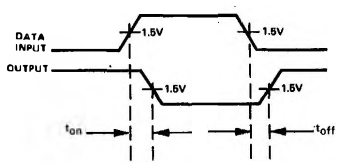
NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each output and the associated data input independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. Refer to AC Test Figures.
10. Not more than one output should be shorted at a time.
11. V_{CC} = 5.25 volts.

AC TEST FIGURES AND WAVEFORMS

PROPAGATION DELAY (DATA TO OUTPUT)



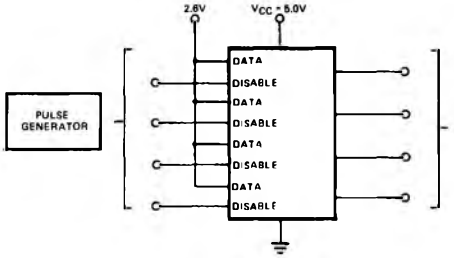


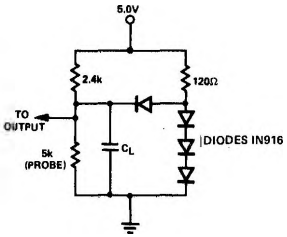
INPUT PULSE:
t_r = t_f = 5ns (10% TO 90%)
FREQ. = 1MHz (50% DUTY CYCLE)
AMP. = 2.6V

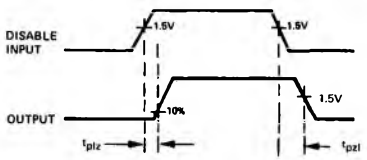
FIGURE 1.

AC TEST FIGURES AND WAVEFORMS (Cont'd)

PROPAGATION DELAY
("0" TO HIGH Z, t_{pLz}; HIGH Z TO 0, t_{pzL})



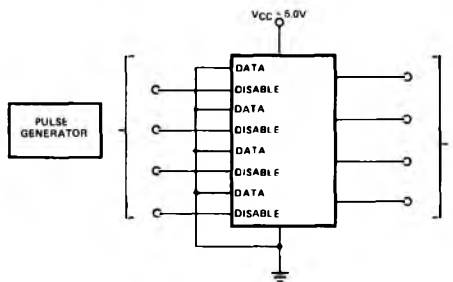


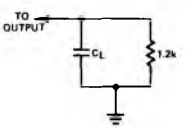


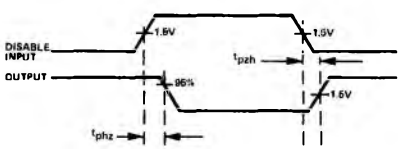
INPUT PULSE:
$t_r = t_f$ = 5ns(10% TO 90%)
FREQ. = 200kHz
AMP = 2.6V

FIGURE 2.

PROPAGATION DELAY
("1" TO HIGH Z, t_{pHz}; HIGH Z to "1", t_{pzH})



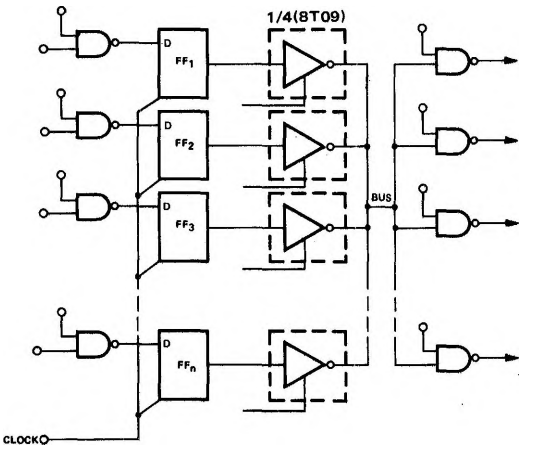




INPUT PULSE:
$t_r = t_f$ = 5ns(10% TO 90%)
FREQ. = 200kHz
AMP = 2.6V

FIGURE 3.

TYPICAL APPLICATION



The above figure illustrates usage of the 8T09 in data processing logic. For example, FF_1 thru FF_n may represent bit X in each of several functions in a minicomputer (accumulators, MQ register, index registers, indirect address registers, etc.). Transfer from any source to any load, including transfers from one register to another, can take place along the single path labeled "BUS".