signetics

TRIPLE LINE RECEIVER WITH HYSTERESIS

8T24

B,W PACKAGES 0°C TO +75°C

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8T24 is a Triple Line Receiver designed specifically to meet the IBM System/360, System/370 I/O Interface Specification (IBM Specification GA 22-6974-0). Each receiver incorporates hysteresis to provide high noise immunity and high input impedance to minimize loading on the driver circuit.

An input voltage of 1.7 volts or more is interpreted as a logical one; an input of 0.70 volts or less is interpreted as a logical zero as is an open circuited input.

The receiver input (R) of the 8T24 will not be damaged by a DC input of +7.0 volts with power on or by a DC input of +6.0 volts with power off in the receiver. The 8T24 will also withstand an input of -0.15V with power on or off.

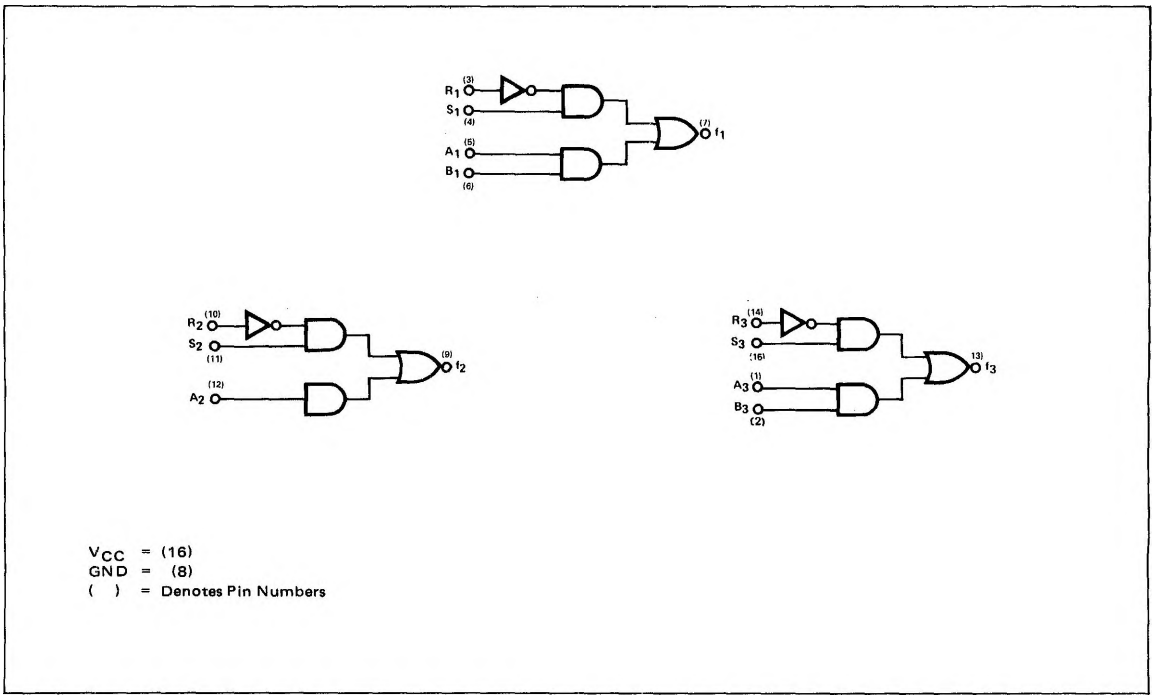
The 8T24 is fully compatible with TTL and DTL systems and operates from a single 5 volt power supply.

FEATURES

- BUILT–IN INPUT THRESHOLD HYSTERESIS*
- HIGH SPEED: $T_{ON} = T_{OFF} = 20ns$ (TYPICAL)
- EACH CHANNEL CAN BE STROBED INDEPENDENTLY
- FANOUT OF TEN (10) WITH STANDARD TTL INTEGRATED CIRCUITS
- INPUT GATING IS INCLUDED WITH EACH LINE RECEIVER FOR INCREASED APPLICATION FLEXIBILITY
- OPERATION FROM A SINGLE +5V POWER SUPPLY

* Hysteresis is defined as the difference between the input thresholds for the "1" and "0" output states. Hysteresis is specified at 0.4V typically and 0.2V minimum over the operating temperature range.

LOGIC DIAGRAM WITH PIN LAYOUT



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V±5%, T_A= 0°C TO +75°C)

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	R	S	A	B	OUTPUTS	
"1" Output Voltage	2.6	3.4		V	1.70V	4.5V	OV	OV	-800μA	7
	2.6	3.4		V	0V	0.7V	OV	OV	-800μA	7
"0" Output Voltage		0.2	0.4	V	0.70V	1.7V	OV	OV	16mA	8
		0.2	0.4	V	0V	0V	1.7V	1.7V	16mA	8
"0" Input Current										
S_n	-0.1		-1.6	mA	0V	0.4V				
A_n	-0.1		-1.6	mA	0V		0.4V			
B_n	-0.1		-1.6	mA				0.4V		
"1" Input Current										
R_n			0.17	mA	3.11V					
R_n			5.0	mA	7.0V					
R_n			5.0	mA	6.0V					9
S_n			40	μA	3.11V	4.5V				
A_n			40	μA			4.5V	OV		
B_n			40	μA			OV	4.5V		

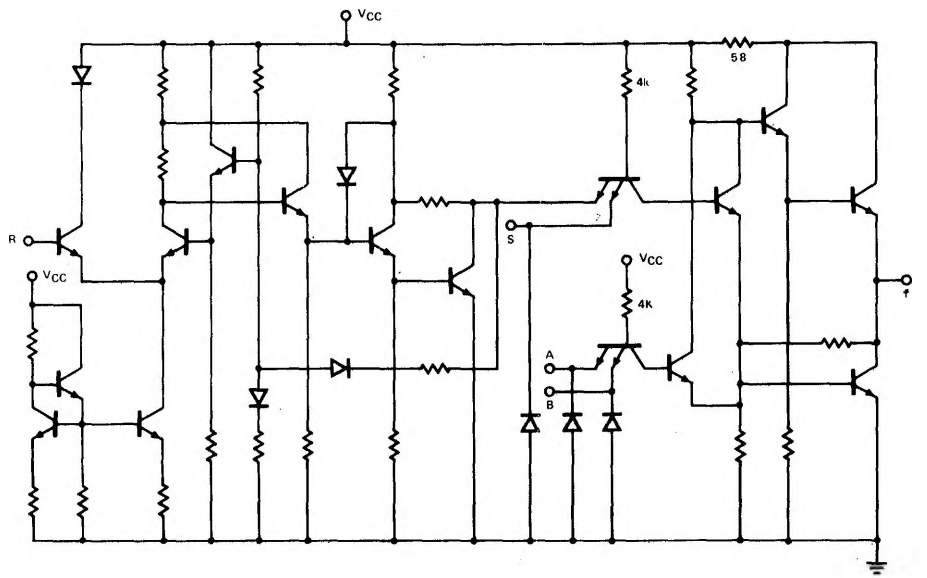
ELECTRICAL CHARACTERISTICS (AT V_{CC}= 5.0v AND T_A = 25°C)

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	R	S	A	B	OUTPUTS	
Turn-On Delay, t_{on}		20	30	nS						13
Turn-Off Delay, t_{off}		20	30	nS						13
Hysteresis	0.2	0.4		V		4.5V	0V	0V		11, 12
Power/Current		315	380	mW						
Consumption		60	72	mA						14
Input Voltage Rating										
S	5.5			V	3.11V	10mA	0V	0V		
A	5.5			V	0V	0V	10mA	0V		
B	5.5			V	0V	0V	0V	10mA		
Output Short Circuit Current	-50		-100	mA	3.11V	0V	0V	0V		10, 14
Input Voltage Rating										
S			-1.5	V		-12mA				
A			-1.5	V			-12mA			
B			-1.5	V				-12mA		

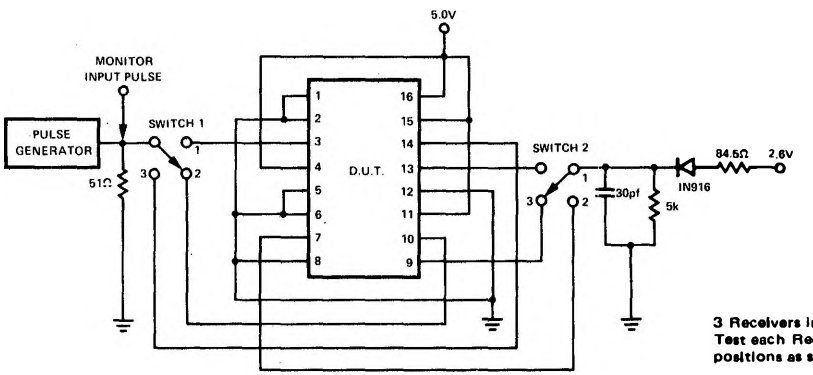
NOTES:

1. All voltage measurments are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Output source current is applied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. V_{CC} = 0.00V
10. Not more than one output should be shorted at a time.
11. Hysteresis is defined as the voltage difference between the R input level at which the output begins to go from "O" to "1" state and the level at which the output begins to go from "1" to "0".
12. See Hysteresis test circuit.
13. Refer to AC test circuits.
14. V_{CC} = 5.25V.

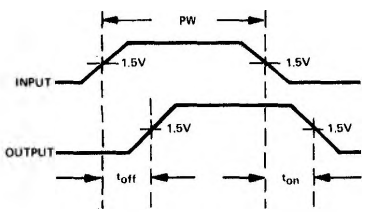
CIRCUIT SCHEMATIC



AC TEST CIRCUIT AND WAVEFORMS



3 Receivers in the package.
Test each Receiver using switch positions as shown in Table I.

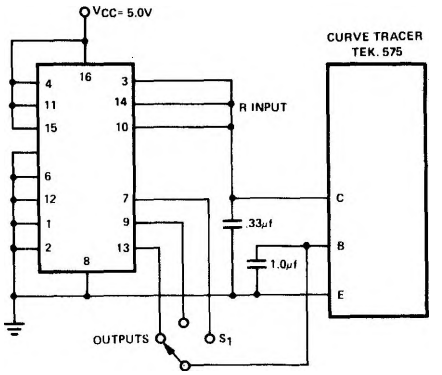


Input Pulse:
Amplitude = 2.6V
Pulse width = 200nS
(50% Duty Cycle)
tr = tf = 5nS (10% to 90%)

TABLE I

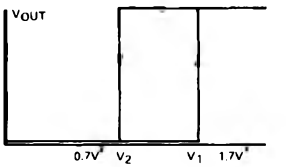
Receiver no.	Position	
	Switch 1	Switch 2
Receiver 1	1	1
Receiver 2	2	2
Receiver 3	3	3

HYSTERESIS TEST CIRCUIT



Verify in each of three (3) positions of S_1 (Figure 1) that the following occurs per Figure 2.

1. V_1 and V_2 must be between 0.7V minimum and 1.7 maximum.
2. Hysteresis = $V_1 - V_2$



TYPICAL APPLICATION