DESCRIPTION

The 8T26 Bus Driver/Receiver contains four pair of inverting logic gates along with two buffered common enable lines.

Both the Driver and Receiver gates have tri-state outputs and PNP inputs. Tri-state outputs provide the high switching speeds of totem-pole TTL circuits while offering the bus capability of open collector gates. PNP inputs reduce input loading to 200μA maximum.

A logic "1" on the Data Enable (D/E) input allows input data to be transferred to the outputs of the Drivers while a logic "0" will force the outputs to a high impedance state and will also disable the PNP resulting in negligible input load current. The Driver gate will sink 40mA of current with a maximum V_{CE} of 0.5V.

The Receiver gates are enabled by a logic "0" on the Receiver Enable (R/E) pin and provide 16mA current sink capability. A logic "1" forces the Receiver outputs to a high impedance state and disables the PNP inputs.

FEATURES

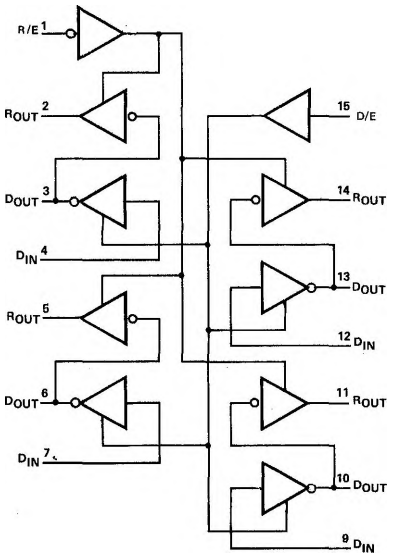
- SCHOTTKY-CLAMPED TTL
- PROPAGATION DELAY = 17ns (MAX.)
- TRI-STATE OUTPUTS
- PNP INPUTS
- 40mA CURRENT SINK CAPABILITY
- SBD* INPUT CLAMPS

*SCHOTTKY-BARRIER-DIODE

APPLICATIONS

- HALF-DUPLEX DATA TRANSMISSION
- ROUTING DATA IN BUS-ORIENTED SYSTEMS
- HIGH CURRENT DRIVERS
- MOS-TO-TTL INTERFACE

LOGIC DIAGRAM



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±5%, T_A = -0°C TO +75°C)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION	NOTES
Input "0" current (All inputs)			-200	μA	V_{in} = 0.4	
Input "1" current D_{in}, D_E, R_E			25	μA	V_{in} = 5.25	
Input (0) Threshold Voltage	0.85			volts		
Input (1) Threshold Voltage			2	volts		
D_{Out} (1) Voltage Pins 3,6,10,13	2.6	3.1		volts	I_{out} = -10mA	7
R_{Out} (1) Voltage Pins 2,5,11,14	2.6	3.1		volts	I_{out} = -2.0mA	7
D_{Out} (0) Voltage Pins 3,6,10,13			0.50	volts	I_{out} = 40mA	8
R_{Out}(0) Voltage Pins 2,5,11,14			0.50	volts	I_{out} = 16mA	8
Output (1) off leakage current			100	μA	V_{out} = 2.6V	
Input clamp voltage			-1.0	volts	I_{in} = -5mA	
D_{Out} short circuit current — Pins 3,6,10,13	-50		-150	mA	V_o = 0 volts	11, 12
R_{Out} short circuit current — Pins 2,5,11,14	-30		-75	mA	V_o = 0 volts	11, 12
Power/Current Consumption			457/87	mW/mA	V_{cc} = 5.25	11

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.00V, T_A = 25°C)

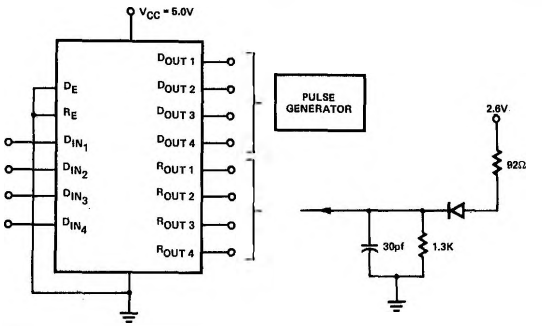
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION	NOTES
Propagation Delay						
D_{Out} to R_{Out} (t_{on})		6	10	nsec		9
D_{Out} to R_{Out} (t_{off})		13	18	nsec		9
D_{In} to D_{Out} (t_{on})		16	20	nsec		9
D_{In} to D_{Out} (t_{off})		16	20	nsec		9
Data Enable to Data Output						
High Z to 0 (t_{pZL})		29	38	nsec		9
0 to High Z (t_{pLZ})		35	43	nsec		9
Receiver Enable to Receiver Output						
High Z to 0 (t_{pZL})		20	30	nsec		9
0 to High Z (t_{pLZ})		10	17	nsec		9

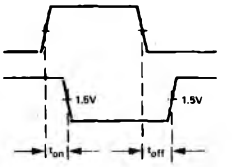
NOTES:

1. All voltage measurements are referenced to the ground terminal.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition:
   "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each output and the associated data input independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. Refer to AC Test Circuits.
10. Manufacturer reserves the right to make design and process changes and improvements.
11. V_{CC} = 5.25 volts.
12. Do not ground more than one output at a time.

AC TEST CIRCUITS AND WAVEFORMS

PROPAGATION DELAY (D_{OUT} TO R_{OUT})

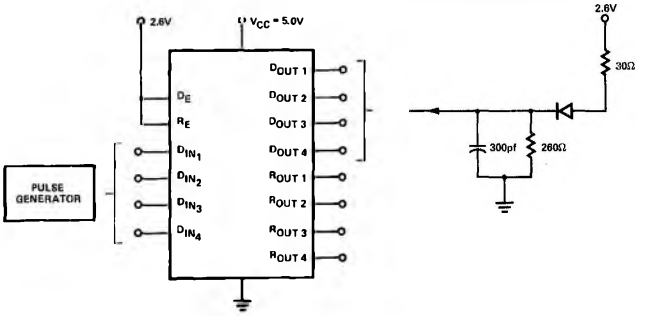


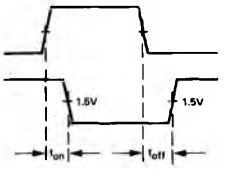


INPUT PULSE:

$t_r = t_f$ = 5ns (10% to 90%)
freq = 10MHz (50% duty cycle)
Amplitude = 2.6V

PROPAGATION DELAY (D_{IN} TO D_{OUT})

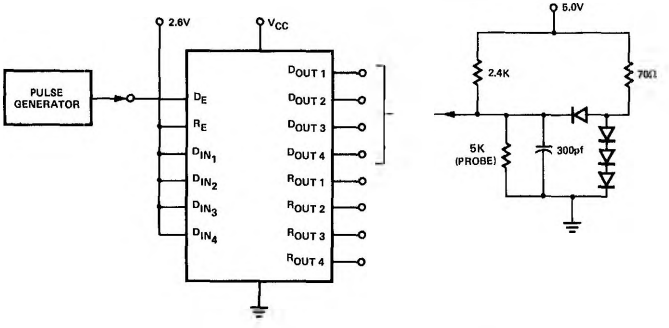


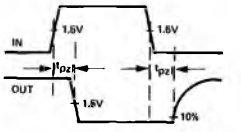


INPUT PULSE:

$t_r = t_f$ = 5ns (10% to 90%)
freq = 10MHz (50% Duty Cycle)
Amplitude = 2.6V

PROPAGATION DELAY (DATA ENABLE TO DATA OUTPUT)

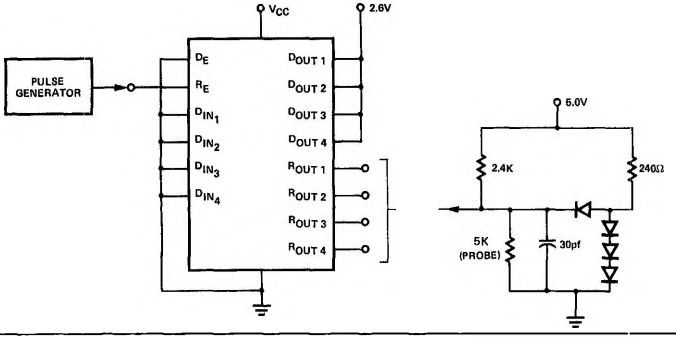


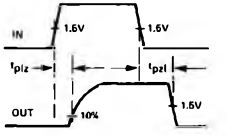


INPUT PULSE:

$t_r = t_f$ = 5ns (10% to 90%)
freq = 5MHz (50% Duty Cycle)
Amplitude = 2.6V

PROPAGATION DELAY (RECEIVE ENABLE TO RECEIVE OUTPUT)





INPUT PULSE:

$t_r = t_f$ = 5ns (10% to 90%)
freq = 5MHz (50% Duty Cycle)
Amplitude = 2.6V

TYPICAL APPLICATIONS