8-BIT LATCHED BIDIRECTIONAL I/O PORT 8T31

FEATURES

- **Dual bidirectional ports**
- **Independent port operation (User-port priority for data entry)**
- **User data input synchronous**
- **At power-up, User-port outputs are high and Microprocessor-port outputs are high-Z**
- **Three-state TTL outputs for high-drive capabilities**
- **Directly compatible with 8X300 Microcontroller**
- **Single +5V supply**

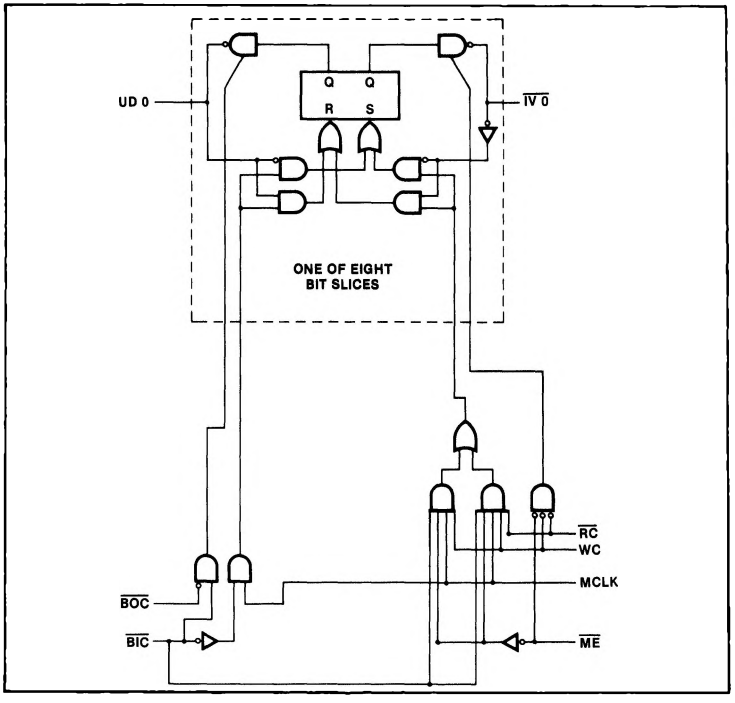
PRODUCT DESCRIPTION

The 8T31 is an 8-bit bidirectional data register designed to function as Input/Output interface elements in microprocessor systems.

Each part contains eight clocked data latches that are accessible from either a *microprocessor* port or a *user* port. Separate I/O control is provided for each port. The two ports operate independently, except that when both are attempting to input data into the data latches, the User port (UD0-UD7) has priority. The master enable (ME) signal enables or disables the microprocessor bus regardless of the state of the other inputs but has no effect on the user bus.

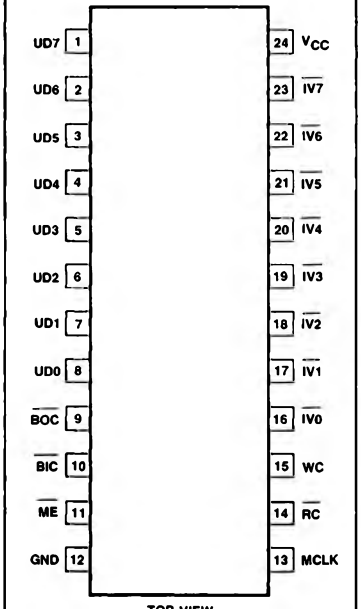
A unique feature of these parts is their ability to start up in a predetermined state. If the clock is maintained at a level of less than 0.8 volts until the power supply reaches 3.5 volts, all bits of the user port will wakeup at a "logic 1" level and those of the microprocessor port will wakeup in the high-impedance state

LOGIC DIAGRAM



PIN CONFIGURATION

N PACKAGE



TOP VIEW

ORDER NUMBERS

N8T31N, N8X31N

8-BIT LATCHED BIDIRECTIONAL I/O PORT 8T31

PIN DESIGNATION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1-8	UD0-UD7	User Data I/O Lines. Bidirectional data lines to communicate with user's equipment	Acitve high three-state
16-23	$\overline{IV0}$-$\overline{IV7}$	Microprocessor Bus. Bidirectional data lines to communicate with controlling digital system.	Active low three-state
10	$\overline{BIC}$:	Input Control. User input to control writing into the I/O Port from the user data lines.	Active low
9	$\overline{BOC}$.	Output Control. User input to control reading from the I/O Port onto the user data lines.	Active low
11	$\overline{ME}$:	Master Enable. System input to enable or disable all other system inputs and outputs. It has no effect on user inputs and outputs.	Active low
15	WC:	Write Command. When WC is high, stores contents of $\overline{IV0}$-$\overline{IV7}$ as data.	Active high
14	$\overline{RC}$	Read Command. When RC is low, data is presented on $\overline{IV0}$-$\overline{IV7}$.	Active low
13	MCLK	Master Clock. Input to strobe data into the latches. See function tables for details	Active high
24	V_{CC}	5V power connection.	
12	GND:	Ground	

Table 1. USER PORT CONTROL FUNCTION

$\overline{BIC}$	$\overline{BOC}$	MCLK	USER DATA BUS FUNCTION
H	L	X	Output Data
L	X	H	Input Data
H	H	X	Inactive

H = High Level L = Low Level X = Don't care

Table 2. MICROPROCESSOR PORT CONTROL FUNCTION

$\overline{ME}$	$\overline{RC}$	WC	MCLK	$\overline{BIC}$	MICROPROCESSOR BUS FUNCTION
L	L	L	X	X	Output Data
L	X	H	H	H	Input Data
X	H	L	X	X	Inactive
X	X	H	X	L	Inactive
H	X	X	X	X	Inactive

USER DATA BUS CONTROL

The activity of the user data bus is controlled by the $\overline{BIC}$ and $\overline{BOC}$ inputs as shown in Table 1.

The user data input is a synchronous function with MCLK. A low level on the $\overline{BIC}$ input allows data on the user data bus to be written into the data latches only if MCLK is at a high level. A low level on the BIC input allows data on the user data bus to be latched regardless of the level of the MCLK input.

To avoid conflicts at the data latches, input from the microprocessor port is inhibited when BIC is at a low level. Under all other conditions the 2 ports operate independently.

MICROPROCESSOR BUS CONTROL

As is shown in Table 2, the activity of the microprocessor port is controlled by the $\overline{ME}$, RC, WC and $\overline{BIC}$ inputs, as well as the state of an internal status latch. $\overline{BIC}$ is included to show user port priority over the microprocessor port for data input.

BUS OPERATION

Data written into the 8T31 from one port will appear inverted when read from the other port. Data written into the 8T31 from one port will not be inverted when read from the same port.

8-BIT LATCHED BIDIRECTIONAL I/O PORT 8T31

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ± 5%, 0°C ≤ T_A ≤ 70°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input voltage:						V
V_{IH}	High		2.0			
V_{IL}	Low				.8	
V_{IC}	Clamp	I_I = 5mA			-1	
Output voltage:		V_{CC} = 4.75V				V
V_{OH}	High		2.4			
V_{OL}	Low				.55	
Input current[1]:		V_{CC} = 5.25V				μA
I_{IH}	High	V_{IH} = 5.25V		<10	100	
I_{IL}	Low	V_{IL} = .5V		-350	-550	
Output current[2]:						mA
I_{OS}	Short circuit	V_{CC} = 4.75V				
	UD bus		10			
	IV bus		20			
I_{CC}	VCC supply current	V_{CC} = 5.25V		100	150	mA

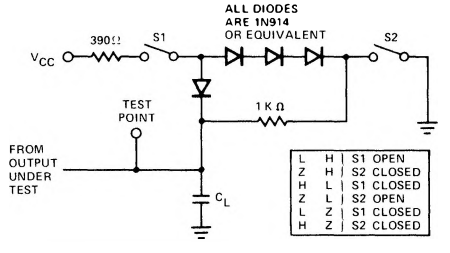
NOTES

1 The input current includes the three-state/open collector leakage current of the output driver on the data lines

2 Only one output may be shorted at a time

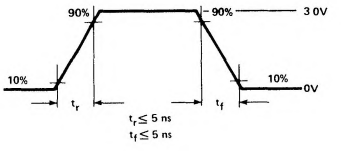
PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT FOR THREE-STATE OUTPUTS

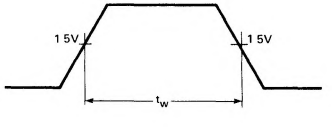


NOTE C_L includes fixture capacitance

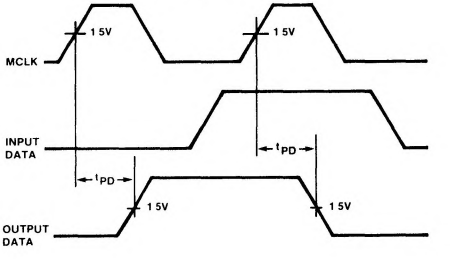
INPUT WAVEFORM



CLOCK PULSE WIDTH



DATA DELAY TIMES
Clock Referenced



AC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, $V_{CC} = 5V \pm 5\%$

PARAMETERS		INPUT	TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
		UD X			25	38	ns
t_{PD}	User data relay[1]	MCLK	C_L = 50pF		45	61	ns
t_{OE}	User output enable	$\overline{BOC}$	C_L = 50pF	18	26	47	ns
		$\overline{BIC}$		18	28	35	ns
t_{OD}	User output disable	BOC	C_L = 50pF	16	23	33	ns
		$\overline{IV}$ X			38	53	ns
t_{PD}	µP data delay[1]	MCLK	C_L = 50pF		48	61	ns
		$\overline{ME}$					
t_{OE}	µP output enable	$\overline{RC}$	C_L = 50pF	14	19	25	ns
		WC					
		$\overline{ME}$					
t_{OD}	µP output disable	$\overline{RC}$	C_L = 50pF	13	17	32	ns
		WC					
t_W	Minimum pulse width	MCLK		40			ns
		$\overline{UD}$ X[3]		15			
		$\overline{BIC}$		25			
		$\overline{IV}$ X		55			
t_{SETUP}	Minimum setup time[2]	$\overline{ME}$		30			ns
		$\overline{RC}$		30			
		WC		30			
		$\overline{UD}$ X[3]		25			
		$\overline{BIC}$		10			
		$\overline{IV}$ X		10			
t_{HOLD}	Minimum hold time[2]	$\overline{ME}$		5			ns
		$\overline{RC}$		5			
		WC		5			

NOTES

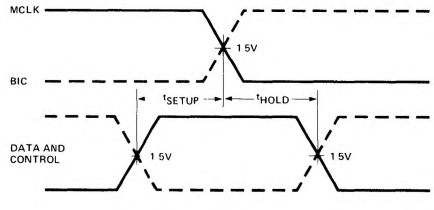
1 Data delays referenced to the clock are valid only if the input data is stable at the arrival of the clock and the hold time requirement is met

2 Set up and hold times given are for "normal" operation $\overline{BIC}$ setup and hold times are for a user write operation $\overline{RC}$ setup and hold times are for an I/O Port select operation $\overline{ME}$ and WC setup and hold times are for a microprocessor bus write operation

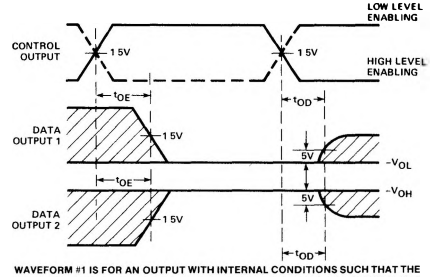
3 Times are referenced to MCLK

VOLTAGE WAVEFORMS

SETUP AND HOLD TIMES



OUTPUT ENABLE AND DISABLE TIMES
(Three-State Outputs)



WAVEFORM #1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW WHEN THE THREE-STATE DRIVER IS ENABLED. WAVEFORM #2 IS FOR THE OPPOSITE CONDITION.