8T31-N,F

DESCRIPTION

The I/O Port is an 8-bit bidirectional data register designed to function as an I/O interface element in microprocessor systems. It contains 8 clocked data latches accessible from either a microprocessor port or a user port. Separate I/O control is provided for each port. The 2 ports operate independently, except when both are attempting to input data into the I/O Port. In this case, the user port has priority.

A master enable (ME) is provided that enables or disables the μP bus regardless of the state of the other inputs, but has no effect on the user bus.

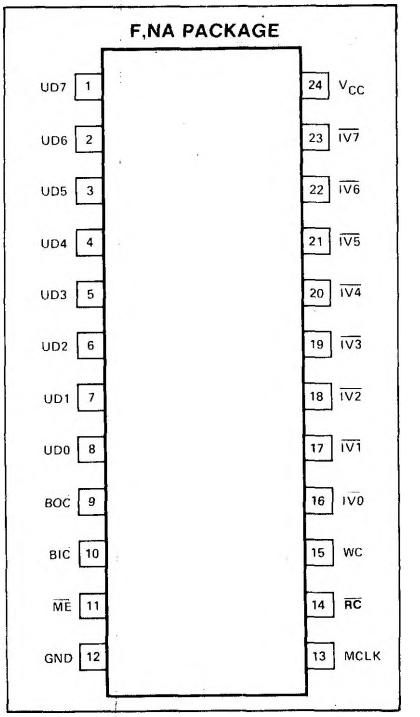
A unique feature of this family is its ability to start up in a predetermined state. If the clock is maintained at a voltage less than .8V until the power supply reaches 3.5V, the user port will always be all logic 1 levels, while the microprocessor port will be all logic 0 levels.

FEATURES

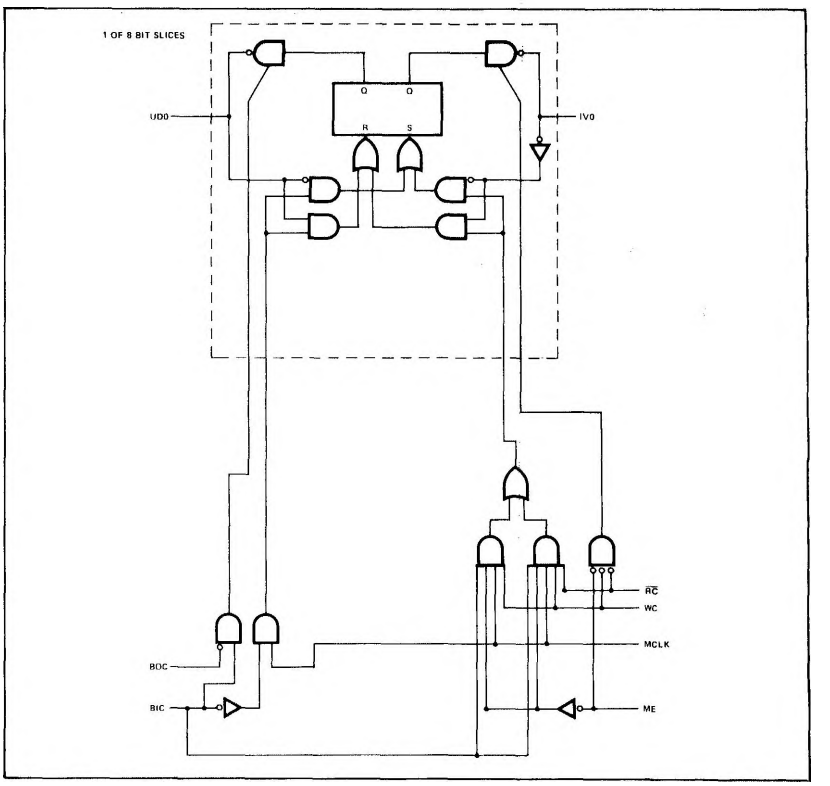
- **Each device has 2 ports, one to the user, the other to a microprocessor. I/O Ports are completely bidirectional**
- **Ports are independent, with the user port having priority for data entry**
- **User data input synchronous**
- **The user data bus is available with tri-state (8T32, 8T36) or open collector (8T33, 8T35) outputs**
- **At power up, the user port outputs are high**
- **Tri-state TTL outputs for high drive capability**
- **Directly compatible with the 8X300 Microcontroller**
- **Operates from a single 5V power supply over a temperature range of 0°C to +70°C**

PIN CONFIGURATION

F,NA PACKAGE



BLOCK DIAGRAM



PIN DESIGNATION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1-8	UD0-UD7:	User Data I/O Lines. Bidirectional data lines to communicate with user's equipment.	Acitve high three-state
16-23	$\overline{IV0}$-$\overline{IV7}$:	Microprocessor Bus. Bidirectional data lines to communicate with controlling digital system.	Active low three-state
10	$\overline{BIC}$:	Input Control. User input to control writing into the I/O Port from the user data lines.	Active low
9	$\overline{BOC}$:	Output Control. User input to control reading from the I/O Port onto the user data lines.	Active low
11	$\overline{ME}$:	Master Enable. System input to enable or disable all other system inputs and outputs. It has no effect on user inputs and outputs.	Active low
15	WC:	Write Command. When WC is high, stores contents of IV0-IV7 as data.	Active high
14	$\overline{RC}$	Read Command. When RC is low, data is presented on IV0-IV7.	Active low
13	MCLK:	Master Clock. Input to strobe data into the latches. See function tables for details.	Active high
24	V_{CC}:	5V power connection.	
12	GND:	Ground.	

$\overline{BIC}$	$\overline{BOC}$	MCLK	USER DATA BUS FUNCTION
H	L	X	Output Data
L	X	H	Input Data
H	H	X	Inactive

H = High Level L = Low Level X = Don't care

Table 1 USER PORT CONTROL FUNCTION

$\overline{ME}$	$\overline{RC}$	WC	MCLK	$\overline{BIC}$	MICROPROCESSOR BUS FUNCTION
L	L	L	X	X	Output Data
L	X	H	H	H	Input Data
X	H	L	X	X	Inactive
X	X	H	X	L	Inactive
H	X	X	X	X	Inactive

Table 2 MICROPROCESSOR PORT CONTROL FUNCTION

USER DATA BUS CONTROL

The activity of the user data bus is controlled by the BIC and BOC inputs as shown in Table 1.

The user data input is a synchronous function with MCLK. A low level on the BIC input allows data on the user data bus to be written into the data latches only if MCLK is at a high level. A low level on the BIC input allows data on the user data bus to be latched regardless of the level of the MCLK input.

To avoid conflicts at the data latches, input from the microprocessor port is inhibited when BIC is at a low level. Under all other conditions the 2 ports operate independently.

MICROPROCESSOR BUS CONTROL

As is shown in Table 2, the activity of the microprocessor port is controlled by the ME, RC, WC and BIC inputs, as well as the state of an internal status latch. BIC is included to show user port priority over the microprocessor port for data input.

BUS OPERATION

Data written into the I/O Port from one port will appear inverted when read from the other port. Data written into the I/O Port from one port will not be inverted when read from the same port.

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ± 5%, 0°C ≤ TA ≤ 70°C unless otherwise specified.

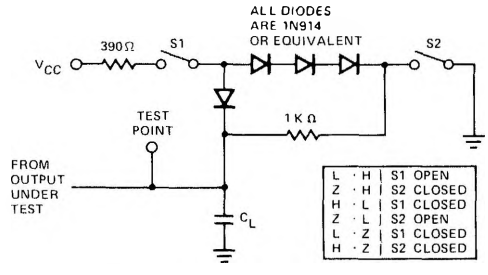
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Min	
	Input voltage					V
V_{IH}	High		2.0			
V_{IL}	Low				.8	
V_{IC}	Clamp	I_I = -5mA			-1	
	Output voltage	V_{CC} = 4.75V				V
V_{OH}	High		2.4			
V_{OL}	Low				.55	
	Input current[1]	V_{CC} = 5.25V				μA
I_{IH}	High	V_{IH} = 5.25V		<10	100	
I_{IL}	Low	V_{IL} = .5V		-350	-550	
	Output current[2]					mA
I_{OS}	Short circuit	V_{CC} = 4.75V				
	UD bus		10			
	IV bus		20			
I_{CC}	VCC supply current	V_{CC} = 5.25V		100	150	mA

NOTES

1. The input current includes the tri-state/open collector leakage current of the output driver on the data lines.
2. Only one output may be shorted at a time.

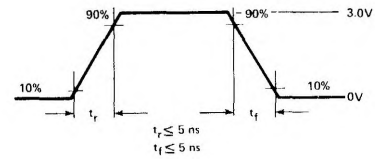
PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT FOR TRI-STATE OUTPUTS

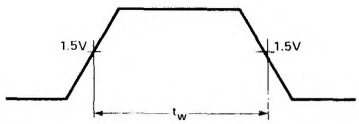


NOTE: C_L includes fixture capacitance.

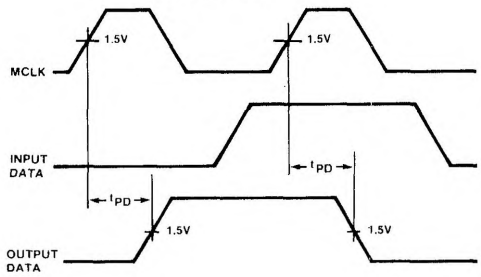
INPUT WAVEFORM



CLOCK PULSE WIDTH



DATA DELAY TIMES
Clock Referenced



AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 5\%$

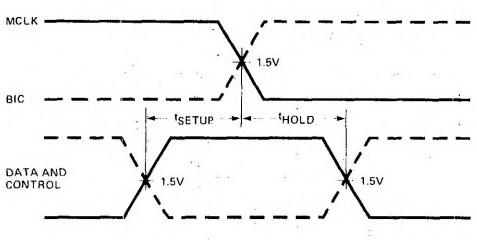
PARAMETER	INPUT	TEST CONDITION	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
t_{PD} User data delay[1]	UDX	$C_L = 50pF$		25	38	ns
	MCLK			45	61	ns
t_{OE} User output enable	BOC	$C_L = 50pF$	18	26	47	ns
t_{OD} User output disable	BIC	$C_L = 50pF$	18	28	35	ns
	BOC		16	23	33	ns
t_{PD} µP data delay[1]	IVBX	$C_L = 50pF$		38	53	ns
	MCLK			48	61	ns
t_{OE} µP output enable	ME RC WC	$C_L = 50pF$	14	19	25	ns
t_{OD} µP output disable	ME RC WC	$C_L = 50pF$	13	17	32	ns
t_W Minimum pulse width	MCLK		40			ns
t_{SETUP} Minimum setup time[2]	UDX[3]		15			ns
	BIC		25			
	IVX		55			
	ME		30			
	RC		30			
	WC		30			
t_{HOLD} Minimum hold time[2]	UDX[3]		25			ns
	BIC		10			
	IVX		10			
	ME		5			
	RC		5			
	WC		5			

NOTES

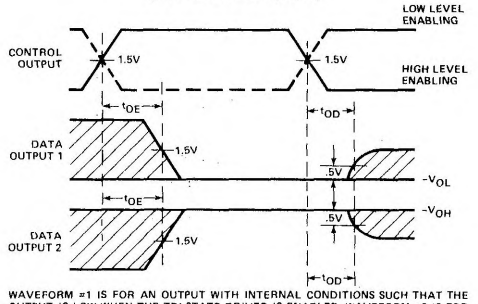
1. Data delays referenced to the clock are valid only if the input data is stable at the arrival of the clock and the hold time requirement is met.
2. Set up and hold times given are for "normal" operation. BIC setup and hold times are for a user write operation. RC setup and hold times are for an I/O Port select operation. ME and WC setup and hold times are for a microprocessor bus write operation.
3. Times are referenced to MCLK

VOLTAGE WAVEFORMS

SETUP AND HOLD TIMES



OUTPUT ENABLE AND DISABLE TIMES
(Tri-State Outputs)



WAVEFORM #1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW WHEN THE TRI-STATE DRIVER IS ENABLED. WAVEFORM #2 IS FOR THE OPPOSITE CONDITION.