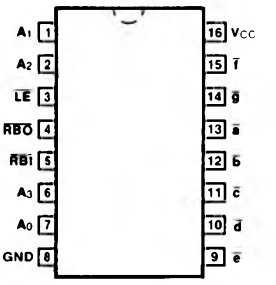
9370

7-SEGMENT DECODER/DRIVER/LATCH

(With Open-Collector Outputs)

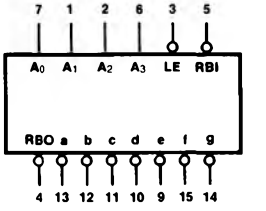
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '70 is a 7-segment decoder driver incorporating input latches and output circuits to directly drive incandescent displays. It can also be used to drive common anode LED displays in either a multiplexed mode or directly with the aid of external current limiting resistors.

- **HIGH SPEED INPUT LATCHES FOR DATA STORAGE**
- **25 mA SINK CAPABILITY TO DRIVE EITHER INCANDESCENT OR COMMON ANODE LED DISPLAYS**
- **HEXADECIMAL DECODE FORMAT**
- **ACTIVE LOW LATCH ENABLE FOR EASY INTERFACE WITH MSI CIRCUITS**
- **DATA INPUT LOADING ESSENTIALLY ZERO WHEN LATCH IS DISABLED**
- **AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING AND/OR TRAILING-EDGE ZEROES**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	PKG TYPE
Plastic DIP (P)	A	9370PC	9B
Ceramic DIP (D)	A	9370DC	6B

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW
$\overline{A_0} - \overline{A_3}$	Address Inputs	2.0/1.0**
$\overline{LE}$	Latch Enable Input (Active LOW)	1.0/1.0
$\overline{RBI}$	Ripple Blanking Input (Active LOW)	1.0/1.0
$\overline{RBO}$	Ripple Blanking as Output (Active LOW)	2.0/2.0
	as Input (Active LOW)	–/2.0
$\overline{a} - \overline{g}$	Segment Outputs (Active LOW)	OC*/25 mA

*OC — Open Collector
**Except Loading is 100 μA @ 0.4 V when $\overline{LE}$ is HIGH.

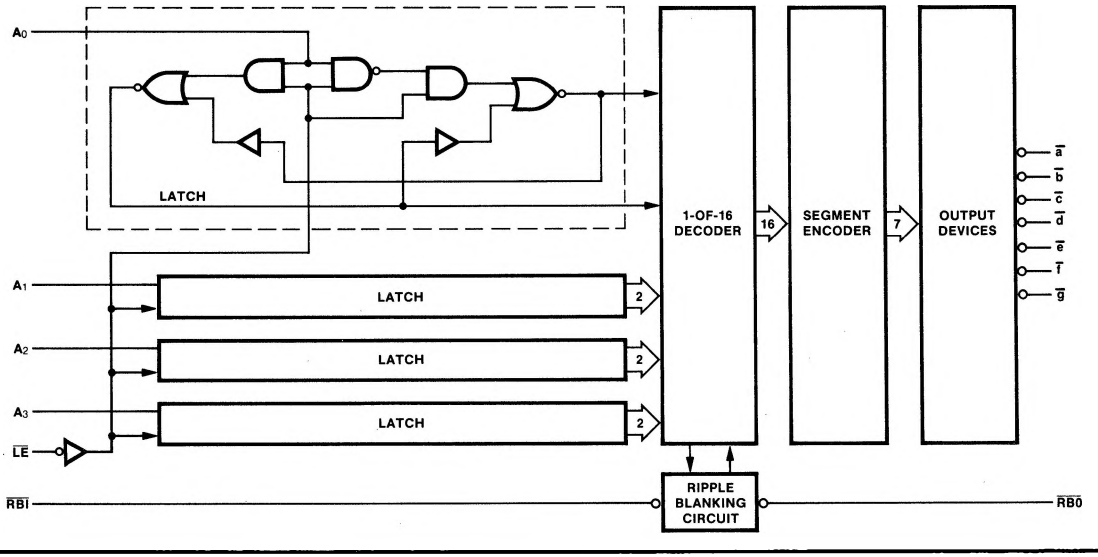
FUNCTIONAL DESCRIPTION — The '70 has active LOW outputs capable of sinking in excess of 25 mA which allows it to drive a wide variety of 7-segment incandescent displays directly. It may also be used to drive common anode LED displays, multiplexed or directly with the aid of suitable current limiting resistors. This device accepts a 4-bit binary code and produces output drive to the appropriate segments of the 7-segment display. It has a hexadecimal decode format which produces numeric codes "0" through "9" and alpha codes "A" through "F" using upper and lower case fonts.

Latches on the four data inputs are controlled by an active LOW latch enable $\overline{LE}$. When the $\overline{LE}$ is LOW, the state of the outputs is determined by the input data. When the $\overline{LE}$ goes HIGH, the last data present at the inputs is stored in the latches and the outputs remain stable. The $\overline{LE}$ pulse width necessary to accept and store data is typically 30 ns which allows data to be strobed into the '70 at normal TTL speeds. This feature means that data can be routed directly from high speed counters and frequency dividers into the display without slowing down the system clock or providing intermediate data storage.

The latch/decoder combination is a simple system which drives incandescent displays with multiplexed data inputs from MOS time clocks, DVMs, calculator chips, etc. Data inputs are multiplexed while the displays are in static mode. This lowers component and insertion costs since several circuits — seven diodes per display, strobe drivers, a separate display voltage source, and clock failure detect circuits — traditionally found in incandescent multiplexed display systems are eliminated. It also allows low strobing rates to be used without display flicker.

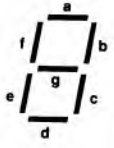
Another '70 feature is the reduced loading on the data inputs when the Latch Enable is HIGH (only 10 μA typ). This allows many '70s to be driven from a MOS device in multiplex mode without the need for drivers on the data lines. The '70 also provides automatic blanking of the leading and/or trailing-edge zeroes in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an 8-digit mixed integer fraction decimal representation, using the automatic blanking capability, 0060.0300 would be displayed as 60.03. Leading-edge zero suppression is obtained by connecting the Ripple Blanking Output ($\overline{RBO}$) of a decoder to the Ripple Blanking Input ($\overline{RBI}$) of the next lower stage device. The most significant decoder stage should have the $\overline{RBI}$ input grounded; and since suppression of the least significant integer zero in a number is not usually desired, the $\overline{RBI}$ input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing-edge zeroes. The $\overline{RBO}$ terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of TTL or DTL gates.

LOGIC DIAGRAM



TRUTH TABLE

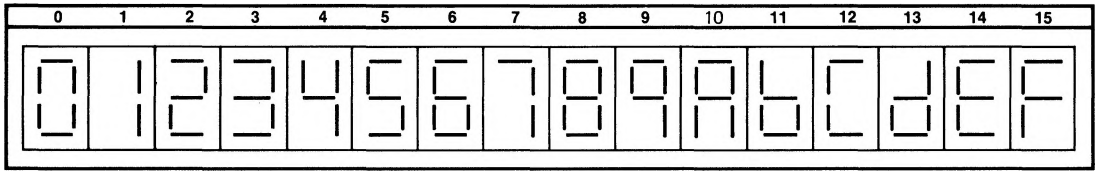
BINARY STATE	INPUTS						OUTPUTS								DISPLAY
	$\overline{LE}$	$\overline{RBI}$	A_3	A_2	A_1	A_0	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	$\overline{RBO}$	
—	H	*	X	X	X	X	◄ STABLE ►							H	STABLE
0	L	L	L	L	L	L	H	H	H	H	H	H	H	L	BLANK
0	L	H	L	L	L	L	L	L	L	L	L	L	H	H	0
1	L	X	L	L	L	H	H	L	L	H	H	H	H	H	1
2	L	X	L	L	H	L	L	L	H	L	L	H	L	H	2
3	L	X	L	L	H	H	L	L	L	L	H	H	L	H	3
4	L	X	L	H	L	L	H	L	L	H	H	L	L	H	4
5	L	X	L	H	L	H	L	H	L	L	H	L	L	H	5
6	L	X	L	H	H	L	L	H	L	L	L	L	L	H	6
7	L	X	L	H	H	H	L	L	L	H	H	H	H	H	7
8	L	X	H	L	L	L	L	L	L	L	L	L	L	H	8
9	L	X	H	L	L	H	L	L	L	H	H	L	L	H	9
10	L	X	H	L	H	L	L	L	L	H	L	L	L	H	a
11	L	X	H	L	H	H	H	H	L	L	L	L	L	H	b
12	L	X	H	H	L	L	L	H	H	L	L	L	H	H	c
13	L	X	H	H	L	H	H	L	L	L	L	H	L	H	d
14	L	X	H	H	H	L	L	H	H	L	L	L	L	H	E
15	L	X	H	H	H	H	L	H	H	H	L	L	L	H	F
X	X	X	X	X	X	X	H	H	H	H	H	H	H	L**	BLANK



*The $\overline{RBI}$ will blank the display only if binary zero is stored in the latches.
**$\overline{RBO}$ used as an input overrides all other input conditions.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

NUMERICAL DESIGNATION



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYBMOL	PARAMETER		93XX Min	93XX Max	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	$\overline{RBO}$	2.4		V	V_{CC} = Min, I_{OH} -80 μA
V_{OL}	Output LOW Voltage	$\overline{RBO}$		0.4	V	I_{OL} = 3.2 mA; V_{CC} = Min
		$\overline{a}-\overline{g}$		0.4		I_{OL} = 25 mA; V_{CC} = Min
I_{OH}	Output HIGH Current, $\overline{a}-\overline{g}$			250	μA	V_{CC} = Max, V_{OUT} = 5.5 V
I_{CC}	Power Supply Current			105	mA	A_1, A_2, A_3, $\overline{LE}$ = Gnd; V_{CC} = Max, Outputs Open
				94		A_0, A_1, A_2, $\overline{LE}$ = Gnd; V_{CC} = Max, Outputs Open

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX C_L = 15 pF, R_L = 500 Ω Min	93XX C_L = 15 pF, R_L = 500 Ω Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{a}-\overline{g}$		75 50	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay $\overline{LE}$ to $\overline{a}-\overline{g}$		90 70	ns	Figs. 3-1, 3-9

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	93XX Min	93XX Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time HIGH or LOW A_n to $\overline{LE}$		30 20	ns	Fig. 3-13
t_h (H) t_h (L)	Hold Time HIGH or LOW A_n to $\overline{LE}$		0 0	ns	Fig. 3-13
t_w (L)	$\overline{LE}$ Pulse Width LOW		45	ns	Fig. 3-9