93L00

93L00 4-Bit Universal Shift Register

Literature Number: SNOS387A

National Semiconductor

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93L00
4-Bit Universal Shift Register

General Description

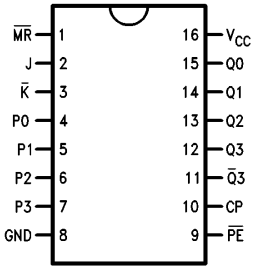
The 93L00 is a 4-bit universal shift register. As a high speed multifunctional sequential logic block, it is useful in a wide variety of register and counter applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers.

Features

- Asynchronous master reset
- J, $\overline{K}$ inputs to first stage

Connection Diagram

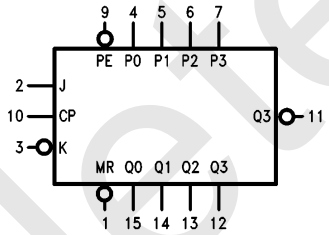
Dual-In-Line Package



TL/F/9576–1

Order Number 93L00DMQB or 93L00FMQB
See NS Package Number J16A or W16A

Logic Symbol



TL/F/9576–2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
$\overline{PE}$	Parallel Enable Input (Active LOW)
P0–P3	Parallel Inputs
J	First Stage J Input (Active HIGH)
$\overline{K}$	First Stage K Input (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$	Master Reset Input
Q0–Q3	Parallel Outputs
$\overline{Q}3$	Complementary Last Stage Output

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	−65°C to +125°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	93L00 (MIL)			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Voltage			−0.4	mA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW, J, $\overline{K}$ and P0−P3 to CP	60 60			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW, J, $\overline{K}$ and P0−P3 to CP	0 0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW, $\overline{PE}$ to CP	68 68			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW, $\overline{PE}$ to CP	0 0			ns
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	38 38			ns
t_w (L)	$\overline{MR}$ Pulse Width LOW	53			ns
t_{rec}	Recovery Time, $\overline{MR}$ to CP	70			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Inputs			20	μA
			CP			40	
			$\overline{PE}$			46	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V	Inputs			−400	μA
			CP			−800	
			$\overline{PE}$			−920	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max				23	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	93L		Units
		C_L = 15 pF		
		Min	Max	
f_{max}	Maximum Shift Frequency	10		MHz
t_{PLH}	Propagation Delay CP to Q_n		35	ns
t_{PHL}			51	
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q_n		60	ns

Functional Description

The Logic Diagrams and Truth Table indicate the functional characteristics of the 93L00 4-bit shift register. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers.

The 93L00 has two primary modes of operation, shift right (Q0 ⟶ Q1) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. When the $\overline{PE}$ input is HIGH, serial data enters the first flip-flop Q0 via the J and $\overline{K}$ inputs and is shifted one bit in the direction Q0 ⟶ Q1 ⟶ Q2 ⟶ Q3 following each LOW-to-HIGH clock transition. The J$\overline{K}$ inputs provide the flexibility of the JK type input for special applications, and the simple D-type input for general applications by tying the two pins together.

When the $\overline{PE}$ input is LOW, the 93L00 appears as four common clocked D flip-flops. The data on the parallel inputs P0–P3 is transferred to the respective Q0–Q3 outputs following the LOW-to-HIGH clock transition. Shift left operation (Q3 ⟶ Q2) can be achieved by tying the Qn outputs to the Pn−1 inputs and holding the $\overline{PE}$ input LOW.

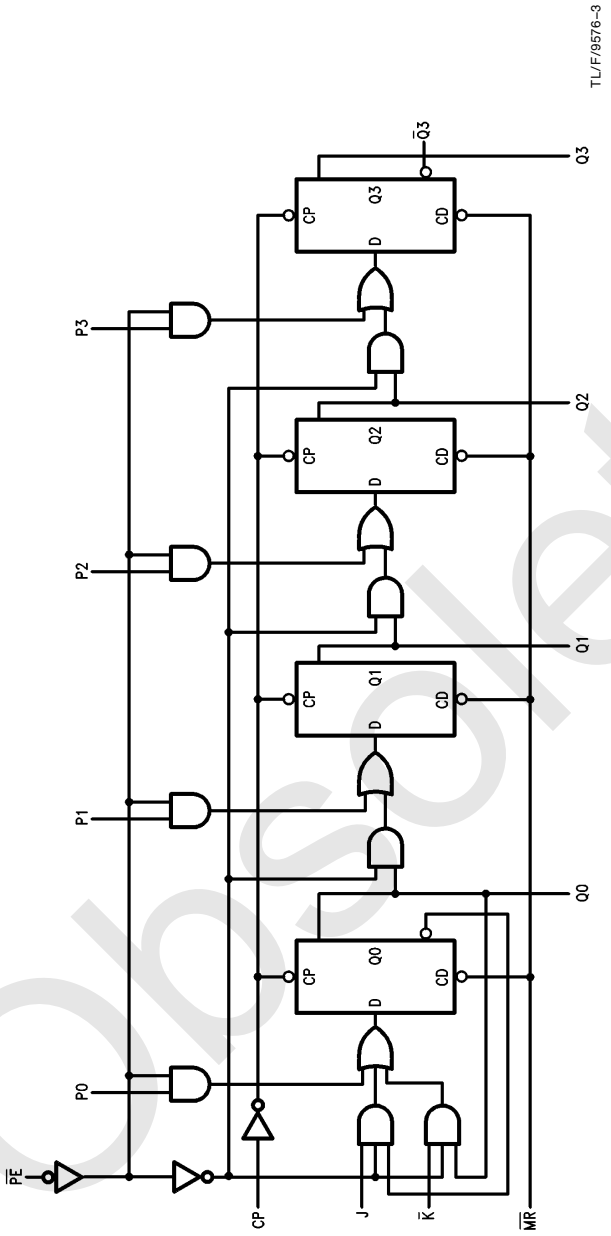
All serial and parallel data transfers are synchronous, occurring after each LOW-to-HIGH clock transition. Since the 93L00 utilizes edge triggering, there is no restriction on the activity of the J, $\overline{K}$, Pn and $\overline{PE}$ inputs for logic operation—except for the setup and release time requirements. A LOW on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs LOW, independent of any other input condition.

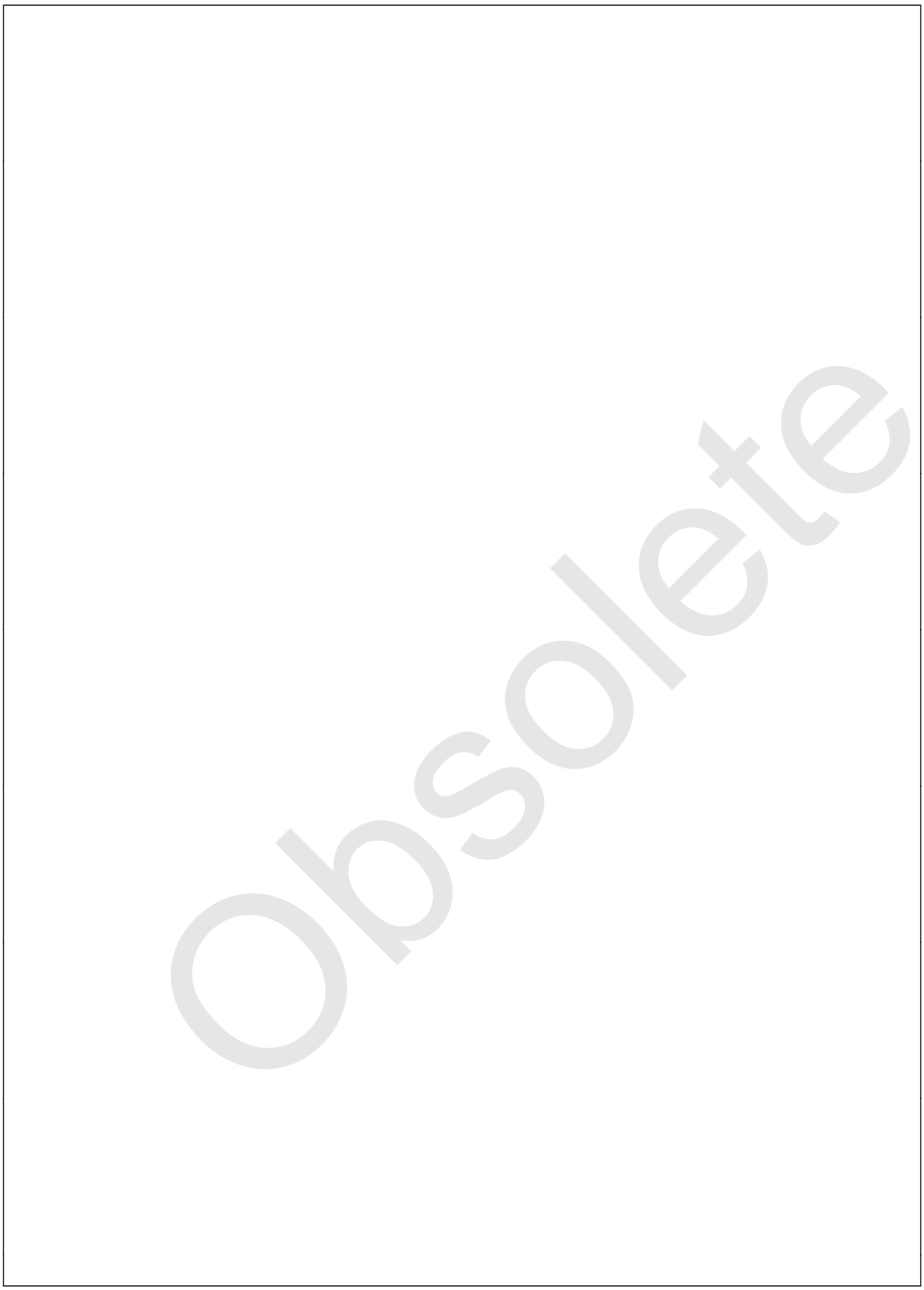
Truth Table

Operating Mode	Inputs ($\overline{MR}$ = H)							Outputs @ t_{n+1}				
	$\overline{PE}$	J	$\overline{K}$	P0	P1	P2	P3	Q0	Q1	Q2	Q3	$\overline{Q}$3
Shift Mode	H	L	L	X	X	X	X	L	Q0	Q1	Q2	$\overline{Q}$2
	H	L	H	X	X	X	X	Q0	Q0	Q1	Q2	$\overline{Q}$2
	H	H	L	X	X	X	X	$\overline{Q}$0	Q0	Q1	Q2	$\overline{Q}$2
	H	H	H	X	X	X	X	H	Q0	Q1	Q2	$\overline{Q}$2
Parallel Entry Mode	L	X	X	L	L	L	L	L	L	L	L	H
	L	X	X	H	H	H	H	H	H	H	H	L

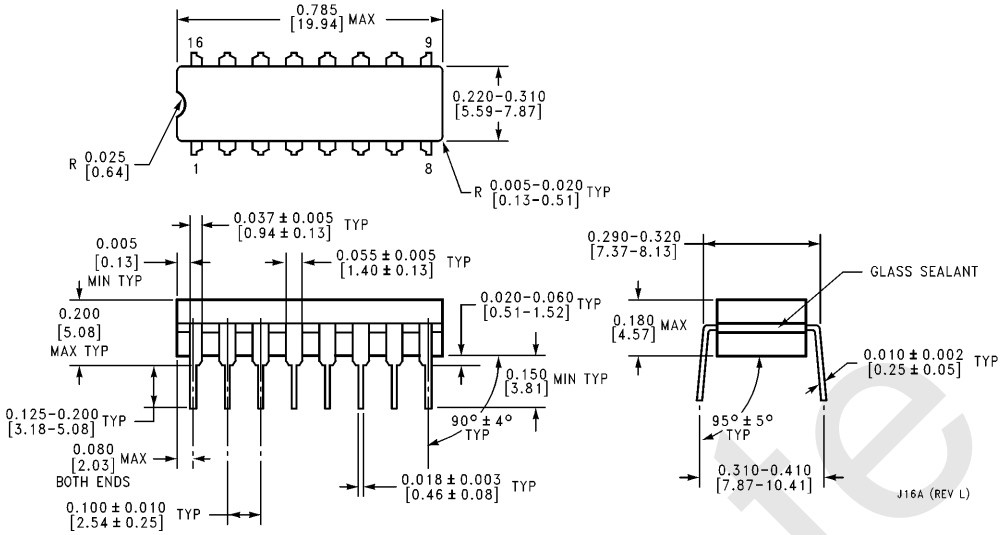
*t_{n+1} = Indicates state after next LOW-to-HIGH clock transition.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



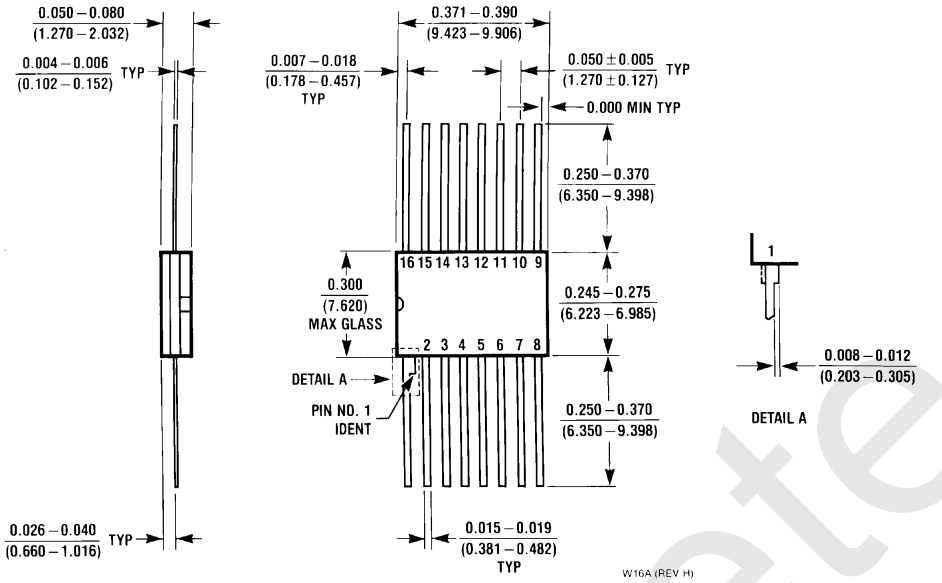

Obsolete

Physical Dimensions inches (millimeters)



16-Lead Ceramic Dual-In-Line Package (J)
Order Number 93L00DMQB
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 93L00FMQB
NS Package Number W16A

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
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National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

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