National Semiconductor

93L24
5-Bit Comparator

General Description

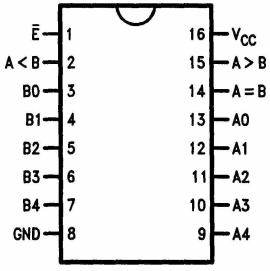
The 93L24 expandable comparator provides comparison between two 5-bit words and gives three outputs—"less than", "greater than" and "equal to". A HIGH on the active LOW Enable Input forces all three outputs LOW.

Features

- Three separate outputs: A<B, A>B, A=B
- Easily expandable
- Active low enable input

Connection Diagram

Dual-In-Line Package



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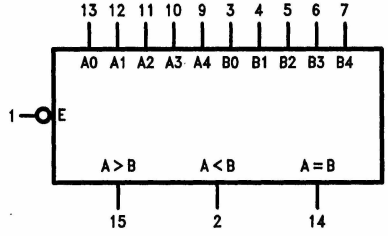
Order Number 93L24DMQB or 93L24FMQB
See NS Package Number J16A or W16A

Logic Symbol



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V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
$\overline{E}$	Enable Input (Active LOW)
A0–A4	Word A Parallel Inputs
B0–B4	Word B Parallel Inputs
A<B	A Less than B Output (Active HIGH)
A>B	A Greater than B Output (Active HIGH)
A=B	A Equal to B Output (Active HIGH)

Truth Table

Inputs			Outputs		
$\overline{E}$	An	Bn	A<B	A>B	A=B
H	X	X	L	L	L
L	Word A = Word B		L	L	H
L	Word A > Word B		L	H	L
L	Word B < Word A		H	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	93L24 (MIL)			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−400	μA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V			−0.8	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max			21	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for test waveforms and output load)

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to A=B; $\overline{E}$ to A<B, A>B		32 35	ns
t_{PLH} t_{PHL}	Propagation Delay An to A>B; Bn to A>B		54 75	ns
t_{PLH} t_{PHL}	Propagation Delay An to A<B; Bn to A<B		70 77	ns
t_{PLH} t_{PHL}	Propagation Delay An or Bn to A=B		100 102	ns

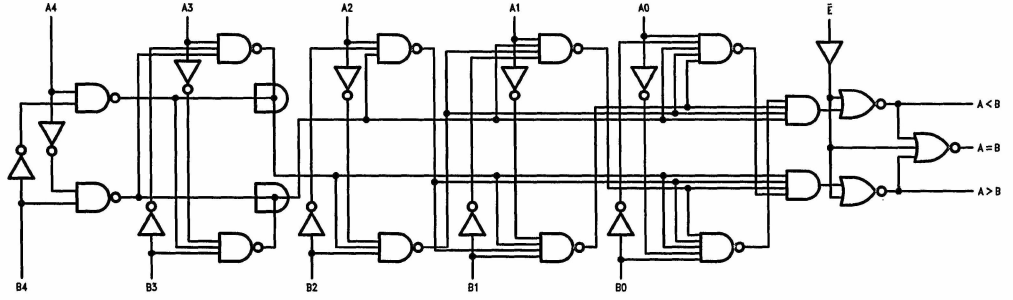
Functional Description

The 93L24 5-bit comparators use combinational circuitry to directly generate "A greater than B" and "A less than B" outputs. As evident from the logic diagram, these ouptuts are generated in only three gate delays. The "A equals B" output is generated in one additional gate delay by decoding the "A neither less than nor greater than B" condition with a NOR gate. All three outputs are activated by the active LOW Enable Input ($\overline{E}$).

Tying the A>B output from one device into an A input on another device and the A< B output into the corresponding B input permits easy expansion.

The A4 and B4 inputs are the most significant inputs and A0, B0 the least significant. Thus if A4 is HIGH and B4 is LOW, the A>B output will be HIGH regardless of all other inputs except $\overline{E}$.

Logic Diagram



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